Optimizing Multi-level Magic State Factories for Fault-Tolerant Quantum Architectures

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We propose a novel technique for optimizing a modular fault-tolerant quantum computing architecture, taking into account any desired space-time trade-offs between the number of physical qubits and the fault-tolerant execution time of a quantum algorithm. We consider a concept architecture comprising a dedicated zone as a multi-level magic state factory and a core processor for efficient logical operations, forming a supply chain network for production and consumption of magic states. Using a heuristic algorithm, we solve the multi-objective optimization problem of minimizing space and time subject to a user-defined error budget for the success of the computation, taking the performance of various fault-tolerant protocols such as quantum memory, state preparation, magic state distillation, code growth, and logical operations into account. As an application, we show that physical quantum resource estimation reduces to a simple model involving a small number of key parameters, namely, the circuit volume, the error prefactors (μ) and error suppression rates (Λ) of the faulttolerant protocols, and an allowed *slowdown factor* (β) . We show that, in the proposed architecture, 10^5-10^8 physical qubits are required for quantum algorithms with T-counts in the range $10^6 - 10^{15}$ and logical qubit counts in the range $10^2 - 10^4$, when run on quantum computers with quantum memory Λ in the range 3–10, for all slowdown factors $\beta > 0.2$.

I. INTRODUCTION

Fault-tolerant compilation of quantum algorithms is especially more complicated than that of classical computer programs because the final physical circuit depends on the specific noise characteristics of the quantum processing unit (QPU). It is commonly understood that the number of non-Clifford logical operations (i.e., the *T*-count of the algorithm) is a good indicator of the approximate cost of running the quantum algorithm. However, assembling the quantum program to run in hours, days, or even months of exact physical circuits on a quantum computer with millions of qubits is much more complicated. Recently, several physical resource estimation platforms have been developed [1, 2] to provide a finer analysis of fault-tolerant quantum computation (FTQC) at utility scale. However, these resource estimators rely on involved bookkeeping of physical qubit counts for various procedures, and therefore are not easily adaptable to alternative circuit decompositions (i.e., beyond Clifford+*T*, e.g., by including Toffoli gates), physical architectures (e.g., for using different state distillation and injection protocols), or the various and possibly very complicated descriptions of the noise of the hardware. This paper is intended to provide a systematic and simple approach to FTQC architecture design, analysis, and optimization.

We present a framework for constructing flexible varieties of FTQC architectures in a modular fashion by allocating dedicated zones across a 2D physical qubit layout for the execution of specific

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(b) Space-time costs for varying quantum hardware



FIG. 1: Space and time cost estimates of an efficient fault-tolerant quantum architecture. (a) Estimates for combinations of *T*-count $T = 10^6$ to 10^{15} and logical data qubits $Q = 10^2$ to 10^4 in a quantum circuit, based on an FTQC model with a quantum memory error prefactor of $\mu_{mem} = 3.8 \times 10^{-3}$ and an error suppression rate of $\Lambda_{mem} = 10$, and a magic state preparation protocol with a linear form with $\mu_{prep} = 1.44 \times 10^{-4}$ and $\Lambda_{prep} = 2.5 \times 10^{-5}$. (b) Estimates for combinations of $\Lambda_{mem} = 3$ to 10 and a magic state preparation protocol with $\Lambda_{prep} = 0$ and $\mu_{prep} = e_{prep} = 10^{-2}$ to 10^{-8} for a circuit with $T = 10^{12}$ and $Q = 10^2$. Each data point corresponds to a slowdown factor β , relative to a serial execution $(\beta = 1)$ of the quantum circuit. A value of $\beta < 1$ reflects a scenario where the magic state factory (MSF) is expanded to meet the magic state consumption rate when parallelizing non-Clifford gates, resulting in faster execution. Conversely, $\beta > 1$ indicates a reduction in MSF size, leading to a longer runtime. While runtime is heavily influenced by the number of non-Clifford gates in the circuit and the MSF size, our estimates demonstrate that quantum computers require between 10^5 and 10^8 physical qubits across all scenarios evaluated.

fault-tolerant protocols. To this end, we view FTQC as the continual production and consumption of various types of expensive quantum resources, such as the production of lower-fidelity logical $|T\rangle$ or $|CCZ\rangle$ states in one zone and their consumption in another zone for obtaining higher-fidelity magic states via a distillation protocol [3]. We consider rotated surface codes as the typical choice of quantum error correction (QEC) codes, and rely on lattice surgery for the execution of entangling gates and seamless routing and teleportation of quantum information across a quantum bus [4, 5].

At utility scale, it is economical to dedicate small numbers of physical code patches as *buffer* registers connecting the FTQC architecture zones to each other. Newly produced resources in one zone are placed in a buffer, where they are fault-tolerantly maintained via continued stabilizer measurements and decoding (quantum memory) for consumption in a subsequent zone. One or many terminal *core processors* consume the final highest-fidelity resources to perform the logical gates of the quantum program. We refer the reader to Section II and Figs. 2 and 3 for further details.

The buffer registers provide several advantages. Practically speaking, they allow for scheduling operations within each zone independently and asynchronously from the other zones. Moreover, since fault-tolerant protocols typically fail with certain non-zero probability, keeping the buffers fully stacked with their associated resource states guarantees that the operations of any dependent zones do not halt since the probability of encountering a completely empty buffer is extremely small. More generally, the oversupply and undersupply of resource states in a buffer can be intentionally used to adjust the space–time trade-offs for FTQC. For example, a magic state factory (MSF) may require many magic state distillation units to keep its buffer fully stacked, while it is possible for a smaller number of distillation units to still be able to fault-tolerantly execute the quantum algorithm if some slowdown caused by occasionally empty buffer registers can be tolerated.

The key idea in this work is to determine the size of each FTQC architecture zone by choosing the number of FTQC protocol units (e.g., 15:1 magic state distillation units, or the like) in that zone in such a way that the supply and demand of the interconnected zones are balanced. This balance, however, can be broken, for the assembly of the program using fewer physical qubits by incurring a longer execution time. However, reducing the (logical) size of the MSF increases the idle time in the core processor, which increases the overall accumulated error rates, potentially requiring larger code distances. Our study provides a detailed analysis of such trade-offs. We model the optimization of space and time as a bi-objective optimization problem in Section III. By solving this optimization problem, we observe that the space and time costs of any FTQC can be efficiently predicted from a small set of key attributes of the quantum program and the quantum computer executing it, and the potential space–time trade-offs for the architecture can be identified.

For clarity we distinguish FTQC compilation and assembly as follows. We assume that the quantum program is given in an intermediate representation (IR) language, also called assembly, after compilation from a higher-level programming environment. Examples of common quantum IR languages are QASM [6] and QIR [7]. However, in this paper, we focus on translation at a lower level from assembly to machine instructions (i.e., QEC rounds and decoder instructions) performed by an *assembler*. Different IR programs may be transpiled into each other efficiently [4, 5]. Therefore, we assume Pauli-based lattice surgery as our IR of choice. For the assembler, the two relevant attributes of the FTQC program are denoted by the Greek small letters α and β , representing the average size of lattice surgeries in the core processor relative to the number of logical qubits and a user-defined slowdown factor within the buffers, respectively. Our empirical studies showed that α is not a significant factor for the assembly process, so we may omit it to obtain an even simpler model depending on only the slowdown factor β . The noise profile of the QPU is also important for the assembler. We observe that this information can be reduced to a small number of parameters for a predictive model of the logical error rates of each FTQC protocol, namely μ and Λ , respectively representing the logical error prefactor and suppression rate of the protocol. Prior literature has used $\Lambda = \Lambda_{\rm mem}$ to quantify the performance of the quantum hardware in a fault-tolerant quantum memory experiment on a single surface code patch [8]. $\Lambda_{\rm mem}$ describes the asymptotic multiple of improvement in the logical fidelity of the QEC code when increasing its distance by 2. More comprehensively, a predictive model for the logical error rate of every fault-tolerant protocol can be devised using additional model parameters. Figure 1 provides a summary of the resource estimates for quantum circuits with varying T-counts, logical qubit counts Q, and quantum computers with varying $\Lambda_{\rm mem}$ and first-stage preparation error rate $e_{\rm prep}$.

Overall, the main contributions of our paper are the following:

- A new modular architecture design procedure for FTQC with at least a multi-level MSF and a core processor;
- An optimization framework that decides the size required for the MSF and the code distances of all logical qubits while minimizing space and time costs; and
- A sensitivity analysis of space and time trade-offs for different quantum circuits and quantum computers.

The paper is organized as follows. Section II introduces our proposed architecture. Section III introduces the error models driven from numerical and experimental hardware noise data. Section IV formalizes the bi-objective optimization problem to be solved and the optimization framework we used to solve the problem. Section V presents our numerical results for trading resource estimations on varying quantum circuits and quantum hardware noise profiles. Finally, Section VI offers concluding remarks.

II. THE FAULT-TOLERANT ARCHITECTURE

We assume rotated surface codes as our QEC scheme of choice and assume that the program to be run is transpiled to multi-qubit Pauli rotations of the angles π , $\pi/2$, and $\pi/4$ for Clifford operations, and $\pi/8$ for non-Clifford operations [9, 10]. These Pauli rotations are in turn implemented using fault-tolerant lattice surgery [4, 5, 11]. A core processor is designed to sequentially perform multi-qubit, long-range entanglements for sets of $\pi/8$ Pauli rotation measurements using auxiliary qubits to connect all the logical qubits required by a given logical operation. The core (see Section II A) is connected to an external multi-level MSF as detailed in Section II B that supplies high-fidelity magic states required for the implementation of these logical operations.

For simplicity, we use an architecture with a single core processor and single MSF as our working example, although our analysis can be directly applied to more-sophisticated architectures with zones for creating other resource states such as the Toffoli [12] and doubly controlled Z (CCZ) [3] magic state distillation units. Moreover, if a quantum algorithm uses a particular rotation angle frequently, a dedicated zone for specific rotation angles can be allocated. It may also be favourable to use distillation protocols that produce more magic states at the cost of a smaller increase in fidelity. Lastly, it might be useful to use dedicated zones for quantum subroutines such as QROM or arithmetic.

A. The Core Processor

The core processor is the central component of the architecture, where logical operations are performed on the logical qubits. It comprises two key elements: the memory fabric and a buffer. The memory fabric is responsible for storing the quantum information required by the computation and performing its logical operations. We follow the fast block layout of Ref. [5], where logical qubits are arranged in two-tile, two-qubit data patches connected to a quantum bus using a square arrangement for performing lattice surgery. This is a time-efficient layout as all Pauli operators—X, Z, and Y being the combination of both—are directly accessible by the quantum bus. In an exact square arrangement, the Q logical qubits requested in the algorithm would require a space of $2Q + \sqrt{8Q} + 1$ tiles plus the tiles required for the buffer space. To save on space, we shorten the last column when $\sqrt{Q/2}$ is not an integer.

The buffer stores the resources prepared in the external MSF and holds them until they are consumed by the $\pi/8$ rotations. The buffer is used to simplify access to magic states so that the memory fabric does not have to directly interface with the MSF. It allows the execution of auto-corrected $\pi/8$ rotations in a single time step, while receiving and preparing new magic states in parallel following the protocol suggested in Ref. [5]. It includes spaces dedicated for magic state growth and storage, which are used for expanding magic states to larger code distances and preparing them for consumption, respectively.

An example layout of the core processor is shown in Fig. 2 for a circuit requiring 18 logical qubits to store its data. The example shows multiple storage and growth units to provide robustness against fluctuations in demand, resulting from parallelization of $\pi/8$ rotations, and production, resulting from distillation failures. More connection points between the memory fabric and the buffer can be added to allow greater parallelization of operations. We note that if the production rate of magic states in the MSF is slower than the consumption rate of magic states in the memory fabric, extra storage capacity is not required; therefore, the buffer space can be reduced in size.



FIG. 2: Example layout of the core processor. The memory fabric is composed of Q = 18 logical qubits distributed in nine two-tile, two-qubit data patches (shown in purple) surrounded by bus qubits (green), while the buffer is composed of magic state storage patches (yellow) dedicated to storing magic states produced in the MSF. This storage space is designed to allow auto-corrected $\pi/8$ rotations by connecting the storage qubits to an ancillary qubit (pink) using lattice surgery in parallel to the lattice surgery used to connect the data patches to the magic state consumed. Magic state growth units are also presented to allow magic state expansion if magic states produced are of a different size than is required.

B. Magic State Factory

The MSF is a module of the fault-tolerant architecture dedicated to the production of highfidelity magic states required to implement the $\pi/8$ rotation gates. Magic states are initially prepared using physical operations in a magic state preparation unit. As these are highly errorprone states that most likely have fidelities below those required for fault tolerance, rounds of magic state distillation are performed using magic state distillation units, where the magic states at one particular level are consumed to create higher-fidelity magic states. Once ready, the magic states distilled are expanded to a larger code distance, if required, in magic state growth units, and transferred to a distillation unit in the next level. When magic states reach the required fidelity, the distillation process has been completed and the magic states created at the highest distillation level are sent to the core processor to be consumed when performing the $\pi/8$ rotation gates. Figure 3 shows an example of the architecture described.

The entire process of magic state distillation is a logical protocol that enables the consumption of lower-fidelity magic states to produce a smaller number of higher-fidelity magic states with some probability of success. There are several such protocols with varying trade-offs between them, such as length, the amount of increase in fidelity, the number of required input magic states, and the number of output magic states [13–15]. However, most known protocols are created using specific error correction or detection protocols in order to reduce the probability of specific types of errors.

Since magic state distillation protocols are performed on logical qubits, each protocol must be performed at a specific code distance. Furthermore, since operations on the logical qubits are faulty, there will be a term in the output fidelity of the magic states dependent on this code distance. In general, this term can be decreased by increasing the code distance at which the magic state distillation operates, but there is generally a trade-off between decreased Clifford



FIG. 3: Architecture of the MSF and its interface with the core processor buffer. Magic states are first prepared using dedicated preparation units following a preparation protocol. They are then dispatched to a buffer where they remain until being requested by its corresponding distillation unit. The higher-fidelity magic states are prepared in the distilling ports of these units. Once ready, they proceed to growth units dedicated to a next-level distillation unit. The process repeats until the highest level sends a magic state to the core processor. In this example, two distillation levels are used, composed of four and two distillation units each from lowest to highest.

errors and increasing numbers of physical qubits operating in a given magic state distillation unit. While it is difficult to theoretically determine the additional error these faulty operations cause, numerical studies can be used to determine how the error rates in the Clifford operations affect the outputs [11].

As a good example that is used as a testbed throughout this paper, the 15:1 distillation protocol [13] uses 15 lower-fidelity magic states and produces a single higher-fidelity magic state. An analysis of this distillation protocol shows that if the input error rates of the magic states are $e_{\rm in}$ and the logical error rates of the individual logical gates are $e_{\rm mem}$, then the output error is bounded by $O(e_{\rm in}^3 + e_{\rm mem})$ from the distillation protocol. From this, one can determine the output fidelity of a single magic state distillation unit given the input fidelities and code distances. Additionally, it is possible to approximate the probability of a successful distillation for this protocol using numerical simulations [11]. Figure 3 shows an architecture for the 15:1 protocol customized to run in 13 logical operations, accounting for 11 gates, one cycle for correction, and one cycle for emptying the distillation port, at a given code distance. This architecture requires at least 28 surface code tiles, much more than the five logical qubits required for the protocol itself.

The very first level of the multi-level MSF consumes logical magic states prepared from physical non-Clifford states that are fault-tolerantly grown to the logical state of a full surface code patch. These protocols generally involve the creation of a physically relevant state (such as a physical magic state), and then the injection of this magic state into a larger quantum error-correcting code [16, 17]. The result is a magic state of fidelity e_{prep} at a specified code distance. Different protocols require different physical operations, and have different time scales, but most require

 $\sim 1-2$ logical cycles, where a logical cycle requires *d* rounds of QEC at the final code distance *d*. The physical execution of the protocols on a 2D layout causes additional error to be accumulated which can also be numerically estimated. At the end of the process, we obtain the error rate $e_{\rm in}$ for the initial level of magic state distillation.

Although distillation levels can be encoded using the same code distances, it is more space efficient to use different encodings for the logical qubits at different levels, usually in increasing order. Therefore, a *growth protocol* must be used between the MSF levels to increase the code distance of the magic states to match the distance of the next distillation level or that of the core processor. These growth protocols operate similarly to the preparation protocols, in which a state encoded in a smaller state is surrounded by additional qubits in specific states, followed by QEC rounds in the grown patch. These growth protocols generally have a small probability of failure, and these probabilities can nevertheless be numerically estimated.

As magic state distillation is a probabilistic procedure, and thus each distillation unit has some chance of not outputting a state, our proposed architecture also includes a buffer register where magic states can remain idle while waiting to be consumed. In this manner, we can reduce the probability of no magic state existing when one is needed. These zones essentially need only to be a single logical tile where the magic state can sit, but having access to the tiles to both load and unload the magic states means they should generally be lined up. Additionally, when magic states interact with the memory fabric, we typically also need access to specific ancillary tiles to facilitate the logical operations that utilize magic states, so these additional ancillary regions are located near the buffer registers to decrease the required logical runtimes of operations involving magic states (see Fig. 3).

III. HARDWARE ERROR MODELLING

Designing the fault-tolerant quantum architecture described requires solving a bi-objective optimization problem that balances minimizing the allocated space (i.e., the physical qubits required) and time (i.e., the runtime for circuit execution) under a given error budget. The decisions to be made are related to sizing the components of the architecture—specifically, the core processor and the MSF—in such a way that both objectives are optimized while ensuring fault tolerance.

The assembler receives an overall error budget for the execution of a given quantum circuit composed of multi-qubit $\pi/8$ rotation gates. This error budget is then distributed between errors that arise in the execution of quantum operations in the core processor, E_{core} , and in the production of magic states in the MSF, E_{msf} . Therefore,

$$E_{\rm core} + E_{\rm msf} \le E. \tag{1}$$

In this section we show how the errors of the code processor and the MSF are modelled and predicted. Although generalizing our models and methods for more-complex architectures is a straightforward task, we present them considering that similar distillation units (e.g., layout and protocol) are used across all levels of the MSF for simplicity. A table summarizing the definition of all variables and parameters used by our error models is given as Appendix A.

A. Core Processor Errors

In the core processor, the quantum algorithm operates on Q logical qubits to execute T non-Clifford gates (i.e., $\pi/8$ Pauli rotations) over a makespan of K logical cycles. The cycles are divided into *active cycles*, where at least one non-Clifford gate is performed in the memory fabric as determined by a compilation procedure, and *idling cycles*, where the data qubits in the memory fabric must be preserved through error correction while waiting for resources (e.g., magic states).

During active cycles, lattice surgeries connect magic states from the buffer to the data qubits to perform the auto-corrected non-Clifford gates scheduled for that cycle. Lattice surgeries used to send magic states from the growth units to the buffers are also considered, although they are performed in previous cycles, either active or idling ones. Each of these lattice surgeries require performing a logical operation involving faulty logical qubits. The error probability for all lattice surgeries required to perform an operation with index $i \in \{1, \ldots, T\}$ is denoted as $e_{\text{surg},i}$, and depends on the size and structure of the lattice surgeries performed [18].

Logical data qubits containing valuable quantum information in the core that are not engaged in active operations must always be protected using rounds of parity checks either during active or idling cycles, which also contribute to the error accumulation. The *idling volume* is defined as

$$V_{\text{idle}} = KQ - \sum_{i=1}^{T} q_i, \qquad (2)$$

where KQ represents all locations where a logical error can occur when protecting idling qubits, and q_i is the number of logical data qubits involved in each non-Clifford gate, which is subtracted from the total to avoid double-counting of the data qubits that are actively involved in a lattice surgery.

The probability of having at least one error when performing all logical operations for idling in the core processor is $1 - (1 - e_{\text{mem,core}})^{V_{\text{idle}}} \approx V_{\text{idle}} e_{\text{mem,core}}$, where $e_{\text{mem,core}}$ is the error rate of the logical qubits in the core processor. Consequently, the approximate total accumulated errors in the core processor from active and idling operations is

$$E_{\text{core}} = V_{\text{idle}} e_{\text{mem,core}} + \sum_{i=1}^{T} e_{\text{surg},i}.$$
(3)

The above formula can be approximated as

$$E_{\rm core} = V_{\rm idle} e_{\rm mem, core} + T e_{\rm cliff, core}.$$
(4)

where α is the average number of patches in all lattice surgeries in the compiled program and $e_{\text{cliff,core}}$ represents the average error rates of all the multi-qubit lattice surgeries in the core. This approximation disregards the varying shapes of different lattice surgeries.

An alternative further simplification is to only use quantum memory error rates. To this end we define the *active volume* of a compiled program as

$$V_{\rm act} = (2Q + \sqrt{8Q} + 26)\alpha T,\tag{5}$$

where $(2Q + \sqrt{8Q} + 26)$ refers to the number of logical qubits in the core, and α is the average size (i.e., number of surface code patches) of the lattice surgeries in the program. This results in the approximation

$$E_{\rm core} \approx (V_{\rm idle} + V_{\rm act}) e_{\rm mem, core}.$$
 (6)

We assume that the assembler has access to the logical error rates of the QEC codes (at high distances). This information may be provided directly by experiments on the quantum hardware. Alternatively, a predictive (parameterized) model $f_{\rm mem}$ can be regressed from numerical simulations

(a) Most probable quantum memory errors



FIG. 4: Shortest-length undetectable errors in FTQC protocols determine the leading factors of the predictive error models. (a) For quantum memory experiments both X and Z type errors land on boundaries of area rd for r rounds of stabilizer measurements. (b-d) For mult-qubit surgeries, no extra rounds of QEC is assumed at the split and the pre-merge phases. (b) Shortest-length error strings of the X-type have a cross section of area O((2d+b)r). (c) Since no distinct pre-merge rounds are assumed, the area of the boundaries of the shortest-length Z-type errors grows as O(d). (d) The degeneracy of the shortest-length undetectable time-like errors scales with the area of the measured bus, db.

at low distances using efficient stabilizer circuit simulators [19, 20]. To summarize, for a core processor of distance d_{core} we have

$$e_{\rm mem,core} = f_{\rm mem}(d_{\rm core}). \tag{7}$$

(b) Most probable X-type errors in surgery

For a quantum memory experiment of distance d involving r QEC rounds, we use

$$f_{\rm mem}(d,r) = \mu_{\rm mem} dr \Lambda_{\rm mem}^{-\frac{d+1}{2}} \tag{8}$$

as our model, where the error prefactor μ_{mem} and the error suppression rate Λ_{mem} are fitting parameters. The error suppression rate Λ_{mem} represents the reduction in the logical error rate when increasing the code distance by two. We expect $\Lambda_{\text{mem}} > 1$ for the surface code below threshold [8, 18, 21]. The exponential suppression with base Λ represents the length (d+1)/2 of the most probable error strings, and the coefficient d^2 accounts for the multiplicity of these error strings, governed by the area of the cross section of the code bulk with error strings of either X or Z type as shown in Fig. 4a.

Similarly, the Clifford error rates e_{cliff} can be approximated using stabilizer circuit simulations at low distances and extrapolated to higher distances. A model for the multi-qubit surgery errors can be extracted from a similar argument involving the shortest length errors in the bulk as shown in Fig. 4. Note that an area law does not apply to all error string types [22]. For example, in an XX surgery between two logical qubits involving r QEC rounds and a bus patch of length b, the error model is

$$f_{\text{cliff}}(d,b,r) = \mu_X(2d+b)r\Lambda_X^{-(d+1)/2} + \mu_Z d\Lambda_Z^{-(d+1)/2} + \mu_T db\Lambda_T^{-(r+1)/2},\tag{9}$$

since the X-type errors have boundary surfaces of areas r(2d + b) (see Fig. 4b), the Z-type errors grow with the length of the boundary edges shown in Fig. 4c and therefore contribute to a linear



FIG. 5: The effect of buffer and decoder delays on surgery fidelities. In core processor surgeries, a teleportation is implemented involving a magic state (the left code patch) and data qubits (represented by the right code patch). The magic state incurs a delay τ_b in the buffer, which in the space-efficient steady flow scenario is one logical cycle on average (i.e., dQEC rounds) before the surgery starts. The data qubit QEC rounds must continue until decoder decisions are available after decoder delay time τ_d .

factor of d in the second term, and the time-like errors of the shortest distance land in a boundary of area bd (Fig. 4d).

For teleporations in our core processor, the teleported state is a magic state that has resided in the buffer for some average expected buffer delay time, τ_b (which is 1 clock cycle for balanced production and consumption rates; see Section IV A for further details). The targets of teleporation are logical data qubit patches in the core processor for which further QEC rounds are executed until the decoder outcome is available. We denote this delay by τ_d . Inclusion of the buffer and decoder delays and assuming an average rate for all types of surgeries changes the above model to

$$f_{\rm surg}(d,b,r) = \mu \left[d(2r + \tau_b + \tau_d + 1) + br \right] \Lambda^{-(d+1)/2} + \mu_T db \Lambda_T^{-(r+1)/2},\tag{10}$$

which still distinguishes time-like and space-like errors but ignores the type of surgery; e.g., XX merge or otherwise (Fig. 5).

B. Magic State Factory Errors

The multi-level MSF described in Section II B produces the high-fidelity magic states required for the $\pi/8$ rotation gates. The probability of errors in the production of magic states affects the overall error rate of execution according to

$$E_{\rm msf} = T e_{\rm msf},\tag{11}$$

where e_{msf} is the error rate of the magic state consumed by each operation in the core.

In the MSF, an iterative process is followed that involves multiple levels of distillation to improve fidelity linked with each other using growth zones. Consider an MSF with L levels: a 0-th level referring to the magic state preparation area, the subset $\{1, \ldots, L\}$ referring to the consecutive distillation levels, and the L + 1-st level being to the core processor. The number of distillation levels $L \in \mathbb{Z}_{\geq 0}$ is to be determined such that the magic state error rate e_{msf} meets the condition in Eq. (1) while satisfying Eq. (11). And the number of qubits used for building the MSF (the space cost) is optimized by choosing an increasing sequence $d_0, d_1, \ldots, d_{L+1} = d_{core}$ of code distances for each of the levels assuming a fault-tolerant code growth protocol is applied within the growth zones to promote code patches of distance d_{ℓ} to those of distance $d_{\ell+1}$. The logical error rate of the magic states provided to the ℓ -th MSF level is denoted by $e_{\text{in},\ell}$ and the error rate of the resulting distilled magic state is $e_{\text{out},\ell}$. Therefore the contribution of the growth zones to the error rates of the magic states between levels is calculated via

$$e_{\text{in},\ell} = g_{\text{grow}}(e_{\text{out},\ell-1}, e_{\text{grow},\ell-1}) = 1 - (1 - e_{\text{out},\ell-1})(1 - e_{\text{grow},\ell-1}), \quad \forall \ell \in \{1, \dots, L+1\},$$
(12)

from simple probabilistic arguments where $e_{\text{grow},\ell-1}$ is the error rate accumulated from the growth procedure performed after level $\ell - 1$.

Similar to Section III A a predictive model (again, to be determined theoretically and regressed numerically or alternatively experimentally) simulating the specific growth protocol is used to infer

$$e_{\text{grow},\ell} = f_{\text{grow}}(d_{\ell}, d_{\ell+1}) \tag{13}$$

as a function of initial and final code distances, d_{ℓ} and $d_{\ell+1}$, in the growth zone. The output magic state error rates $e_{\text{out},\ell}$ are given by a function of the form

$$e_{\text{out},\ell} = g_{\text{dist}}(e_{\text{in},\ell}, e_{\text{cliff},\ell}) \tag{14}$$

which for example for the 15:1 distillation protocol is

$$e_{\text{out},\ell} = 35e_{\text{in},\ell}^3 + 7.1e_{\text{cliff},\ell}$$
 (15)

as per Refs. [5, 11, 23]. The coefficient 35 is driven theoretically [23] however the contribution of surgeries within the ℓ -th distillation circuit is approximated as a numerically driven multiple (7.1 in [24]) of the Clifford error rate $e_{\text{cliff},\ell}$ obtained from the model Eq. (10).

Overall, the magic state error rates of the entire MSF can be calculated recursively as follows:

$$e_{\text{out},0} = e_{\text{in},1} = e_{\text{prep}},\tag{16}$$

$$e_{\text{out},\ell} = g_{\text{dist}}(e_{\text{prep}}, e_{\text{cliff},\ell}), \quad \forall \ell \in \{1, \dots, L\},$$
(17)

$$e_{\mathrm{in},\ell+1} = g_{\mathrm{grow}}(e_{\mathrm{out},\ell}, e_{\mathrm{grow},\ell}), \quad \forall \ell \in \{1, \dots, L-1\},\tag{18}$$

$$e_{\text{in},L+1} = e_{\text{msf}} = g_{\text{grow}}(e_{\text{out},L}, e_{\text{grow},L}).$$
(19)

Here the preparation error rate e_{prep} is estimated from numerical simulation of the fault-tolerant magic state preparation protocol in use at the zeroeth MSF level (i.e., at distance d_0). The numerical behaviour of these protocols as a function of d in the error regimes in which we are interested can be quite distinct. For instance, for some protocols [17, 25], the error rate

$$e_{\rm prep} = f_{\rm prep}(d_0) = \mu_{\rm prep} - \Lambda_{\rm prep} d_0, \qquad (20)$$

with a negative error suppression rate Λ_{prep} , which leads to the error rate increasing linearly with respect to distance. However, more recent protocols [26] exhibit an exponential suppression in their error rates as far as numerical simulations in the regime of practically relevant distances and physical error rates are concerned:

$$e_{\rm prep} = \mu_{\rm prep} \Lambda_{\rm prep}^{-\frac{d+1}{2}}.$$
(21)

In both cases, the starting factor μ_{prep} and the error suppression rate Λ_{prep} are fitting parameters. Other protocols might have different behaviour altogether.

Combining Eqs. (2), (3) and (11) we can rewrite the error budget constraint Eq. (1) as

$$e_{\mathrm{msf}}T + e_{\mathrm{mem},L+1}\left(KQ - \sum_{i=1}^{T} q_i\right) + \sum_{i=1}^{T} e_{\mathrm{surg},i} \leq E.$$
(22)

Therefore, given a compiled quantum circuit with T non-Clifford gates involve Q logical qubits, run (potentially with some parallelization) in K logical cycles, involving q_i qubits in the *i*-th non-Clifford operation, and the hardware error models described above, we can determine the number of distillation levels L, the code distances at each level, and the code distance in the core processor such that Eq. (22) is satisfied.

IV. THE ASSEMBLY PROCESS

In this section we show how the predicted error rates from the previous section are used to decide the sizing of the MSF and all code distances involved.

A. Space and Time Costs

The space and time costs with respect to the architecture depend on the sizes of the core processor and the MSF. Each logical cycle in the makespan K, either active or idling, requires performing d_{L+1} parity checks, each taking a time W determined by hardware characterization for the QEC scheme considered. Therefore, ignoring the warm-up time (i.e., the time needed to start filling the core buffer with high quality magic states), which is negligible for utility-scale quantum circuits, we can calculate the runtime R of the quantum circuit as:

$$R = KWd_{L+1}. (23)$$

Therefore, for a given QPU, R is minimized by reducing the product of the code distance of the core processor d_{L+1} and the makespan K, which is determined based on the production rate of magic states in the MSF and the demand profile for magic state consumption in the core.

A compilation process, such as those described in Refs. [4] and [24], can determine sets of $\pi/8$ rotation gates that can be performed in parallel. The compilation in these studies assumes that magic states are always available to be consumed by all gates scheduled for the same logical cycle. Let a quantum algorithm composed of T non-Clifford gates be represented by $T = \sum_{i=1}^{T_{depth}} t_i$, where T_{depth} determines the minimum number of logical cycles required to execute the algorithm (the shortest possible makespan, $K \leq T_{depth}$), and t_i denotes the maximum number of $\pi/8$ rotations that can be performed in the time step i as determined by a compilation process. Ignoring fluctuations in the demand for magic states, we can define the maximum consumption rate of the core processor as

$$C_{L+1} = \frac{Wd_{L+1}T_{\text{depth}}}{T},\tag{24}$$

since logical cycles would be expected to consume, on average, T/T_{depth} magic states every logical cycle that takes a time Wd_{L+1} .

The production rate of magic states in a factory is determined by the production rate of all distillation units in its uppermost level, that is, D_L . A time-optimal architecture requires

$$D_L \ge C_{L+1}.\tag{25}$$

Different scenarios are observed:

• If $D_L > C_{L+1}$, then the MSF is oversized, which increases the space cost but with no reduction in the time cost, except when the magic state demand is too volatile, since they can be stocked during periods of low demand to avoid a shortage during periods of high demand;

- If $D_L = C_{L+1}$, then the MSF is space efficient to minimize the time cost; and
- If $D_L < C_{L+1}$, then the MSF is undersized, so the circuit takes longer to execute. The added idling time to the makespan K inflates the idling volume V_{idle} , as defined in Eq. (2). Thus, although the number of distillation units in the MSF decreases, the core processor size may increase due to there being a lower error budget availability for the errors accumulated during lattice surgery, as shown in Eq. (3).

To achieve the production rate D_L required for a time-optimal solution, we must ensure that production and consumption rates are balanced over all distillation levels. The production rate of any distillation level $\ell \in \{1, \ldots, L\}$ composed of u_ℓ parallel distillation units for this level is bounded by

$$D_{\ell} \le \frac{u_{\ell} N P}{W d_{\ell} (O+N)},\tag{26}$$

where N is the number of magic states produced in a distillation round, P is the acceptance probability, Wd_{ℓ} is the execution time of each logical operation in the unit, and O is the number of logical cycles required for the distillation round. The parameters N and O are given based on the distillation protocol, the acceptance probability is a function $P = f_{\rm acc}(e_{\rm in,\ell}, e_{\rm mem,\ell})$, and W is based on the hardware characterization. Equality in Eq. (26) is obtained when a steady execution of logical operations is possible due to a sufficient supply of magic states. Given that the consumption rate of magic states by all units in this level is

$$C_{\ell} \le \frac{u_{\ell}M}{Wd_{\ell}(O+N)},\tag{27}$$

a steady flow is possible when $D_{\ell-1} \ge C_{\ell}$, where M is the number of input magic states for the distillation unit. For example in the 15:1 distillation protocol M = 15, N = 1, O = 13, and

$$P = 1 - 15e_{\rm in} - 356e_{\rm cliff}.$$
 (28)

To achieve a space-efficient steady flow, we need to ensure that

$$D_{\ell-1} = C_{\ell}, \quad \forall \ell \in \{1, \dots, L+1\}.$$
 (29)

Combining the previous equations, we obtain the following relations between the number of distillation units and code distances between levels, which are given for the uppermost, intermediate, and lowermost levels, respectively, as

$$\frac{u_L NP}{d_L (O+N)} = \frac{d_{L+1} T_{\text{depth}}}{T},\tag{30}$$

$$\frac{u_{\ell-1}NP}{d_{\ell-1}} = \frac{u_{\ell}M}{d_{\ell}}, \quad \forall \ell \in \{2, \dots, L-1\},$$
(31)

$$D_0 = \frac{u_1 M}{d_1}.\tag{32}$$

In the lowermost level, the magic state preparation rate D_0 is determined based on the preparation unit cycle time according to the magic state preparation protocol implemented.

Solving Eqs. (30) to (32) considering the error budget in Eq. (22) leads to an architecture that approximates the space required to minimize time costs. Space costs are measured by the number of physical qubits required to encode all logical qubits in the layout. The exact number of logical qubits in the core processor is determined as described in Section II A for the memory fabric, while

we consider a buffer with a fixed size of 25 logical qubits (represented in Fig. 2) that guarantees a steady flow of magic states for a circuit with $T = T_{depth}$. And, each logical qubit in the surface code requires $2d^2 - 1$ physical qubits.

For example, in the 15:1 distillation unit layout used in Fig. 3:

- each distillation unit requires 23 logical qubits regardless of its level;
- each distillation unit in all levels but the lowermost still requires 5 dedicated growth units supplying magic states to it, each requiring a space equivalent to a logical qubit with code distance d_{ℓ} ;
- each distillation unit in the lowermost level requires 10 logical qubits for handling the prepared magic states, 3 of which are for preparation units as determined by preliminary experiments using common hardware characterizations; and
- each distillation level ℓ still requires at least $5u_{\ell} + 4$ qubits to connect the distillation units to the upper-level growth units.

Based on these considerations, the total space cost for a time-optimal architecture is approximated as

$$S \approx (2d_{L+1}^2 - 1)(2Q + \sqrt{8Q} + 29) + (2d_1^2 - 1)(41u_1 + 4) + \sum_{\ell=2}^{L} (2d_{\ell}^2 - 1)(33u_{\ell} + 4).$$
(33)

While solving Eqs. (30) to (32) leads to a time-optimal solution, if a distillation unit can meet the requirements to produce higher-fidelity magic states from lower-fidelity ones, only one distillation unit per level is necessary for an MSF to be able to produce magic states at the error rates meeting the condition in Eq. (22). As previously mentioned, an MSF with $u_{\ell} = 1, \forall \ell \in \{1, \ldots, L\}$, may significantly reduce the last two terms in Eq. (33) at the cost of increasing the first one through an increase in d_{L+1} . This trade-off is analyzed in detail in Section V.

B. Our Assembly Method

Although the problem presented in Section III can be solved analytically, the complexity of representing the nested function for the accumulated MSF errors in Eq. (22) and the relations between the decision variables in Eqs. (30) to (32) demand the development of a fast heuristic algorithm to solve the problem. This algorithm generates layouts for the considered architecture under both time-optimal and -suboptimal scenarios.

Since the objective is to balance space and time costs, the slowdown factor β we introduce acts as a target value for the runtime slowdown by choosing an undersized MSF. The number of logical cycles required to run the quantum algorithm is approximated by $K = \beta T$. A time-optimal solution corresponds to the expression $\beta = T_{depth}/T$, while the value $\beta = 1$ leads to a space-optimal solution that leads to approximately no excess idling time for the serial scheduling case. For $\beta > 1$, the MSF must be sized accordingly to estimate the resulting idling time. While the slowdown may not match the value of β precisely due to the discrete nature of distillation units, we adjust Kaccordingly to match the actual slowdown resulting from the MSF size chosen to approximate β .

We now detail the decision-making process for solving the optimization problem described. Note that the parameters α and β are present in Eq. (6) as factors of V_{act} and V_{idle} , respectively. As such, they are set prior to solving the problem to approximate the error rates in the core processor.

1. Set the Core Area's Code Distance

The first decision to be made is to determine the code distance d_{L+1} for the core processor, assuming $E_{msf} = 0$ (i.e., there are no magic state factory errors). The minimum code distance that satisfies Eq. (22) is found by solving the following problem:

$$\min \quad d_{L+1} \tag{34}$$

s.t.
$$(V_{\text{idle}} + V_{\text{act}})e_{\text{mem},L+1} \le E,$$
 (35)

 $d_{L+1} \in \{2k+1 | k \in \mathbb{Z}_+\},\tag{36}$

where V_{idle} , V_{act} , and $e_{\text{mem},L+1}$ are represented by the Eqs. (2), (5), and (8), respectively. Since all the parameters except d_{L+1} are known a priori, this problem is easily solved by gradually increasing d_{L+1} within its feasible space until a feasible solution for the problem is found.

2. Set the First-Level's Code Distance

Once d_{L+1} has been determined, we calculate E_{core} using Eq. (6) and, following Eqs. (1) and (11), we set the magic state error budget according to

$$e_{\rm msf} \le \frac{E - E_{\rm core}}{T}.$$
 (37)

If this error threshold can be achieved without distillation, that is, e_{prep} is below the right-hand side threshold above, the problem has been solved since no distillation is required. Otherwise, we proceed by defining a first distillation level and selecting the code distance d_1 that minimizes the magic state error rate:

$$\min e_{\text{out},1} \tag{38}$$

s.t.
$$P > 0,$$
 (39)

$$d_1 \in \{2k+1 | k \in \mathbb{Z}_+\}.$$
 (40)

Here, the objective function (38) is a function for the magic state output error rate as in Eqs. (14) and (15), and the constraint (39), determined for example by Eq. (28), ensures that the acceptance probability is positive in order to validate the choice. While this problem can be solved using gradient-based methods, the limited solution space affords a quick way of verifying optimality by iterating through code distances while verifying feasibility until the turning point is reached in both functions $e_{out,1}$ and P.

3. Determine the Number of Distillation Levels

Minimizing the number of distillation levels L generally leads to space-efficient solutions by avoiding the overhead of added levels even if they have small code distances. We decide on the number of distillation levels by incrementally adding levels with a code distance of $d_{\ell} = \infty$, which results from the output error bound from the distillation protocol, until the magic state error rate $e_{\text{out},L} \leq e_{\text{msf}}$, considering the accumulated errors described in Section IIIB.

4. Update the Code Distances for All Levels

Once the number of distillation levels has been set, we update the code distances d_{ℓ} for all levels, including the first one. This is because we are not looking to improve the error rate at each level as

much as possible, but instead only to improve it so as to meet the error budget E. Beginning with the first level, we search for the smallest value of d that leads to the error budget being met when updating the error rates in Eq. (19) throughout the distillation process. This iterative process continues until all levels meet the error budget.

5. Determine the Number of Distillation Units

Finally, we determine the number of distillation units, u_{ℓ} , at each level. We first calculate the consumption rate in the core C_{L+1} using Eq. (27) and the maximum production rate D_L of a single distillation unit $u_L = 1$ at the level L based on Eq. (26). Then, the number of distillation units is set to

$$u_L = \left\lceil \frac{\beta D_L}{C_{L+1}} \right\rceil. \tag{41}$$

This process is repeated for each level, with β adjusted based on the production rate of the selected number of units. Thus, when the chosen number of distillation units u_{ℓ} leads to a production rate above the target β , $u_{\ell-1}$ takes into consideration this gap and selects only enough units to approximate the target slowdown rate.

6. Local Search

To further improve the solution, a local search is conducted. The algorithm increases the code distance one level at a time, rebalancing production and consumption rates while recalculating space costs. If an improvement is found, the solution is updated, and the process continues. The search stops when no further local improvements can be found.

V. EXPERIMENTS

We conducted a set of experiments to analyze optimal solutions for the studied problem and to perform a sensitivity analysis on the parameters that were input, including the number of logical qubits (Q), the circuit depth (T), and hardware noise parameters. For simplicity we assumed $e_{\text{cliff}} = e_{\text{mem}}$ and that the quantum memory protocol had r = d rounds everywhere, therefore, the hardware noise parameters were merely the quantum memory error suppression rate (Λ_{mem}), and the preparation error rate (e_{prep}). The experiments did not require much computational power; they should be easily reproducible even on a personal computer. We also assumed the 15:1 distillation protocol with the layout of Fig. 3 were used for all $\forall \ell \in \{1, \ldots, L\}$; therefore, M = 15, $N = 1, P = 1 - 15e_{\text{in}} - 356e_{\text{mem}}, Q = 13$, and $e_{\text{out}} = 35e_{\text{in}}^3 + 7.1e_{\text{mem}}$.

As part of the default settings, we considered the error budget E = 1%. A $\Lambda_{\text{mem}} = 10$ model was simulated using 1QBit's TopQAD software [27], resulting in $\mu_{\text{mem}} = 3.8 \times 10^{-3}$ for the logical error rate model, and $\mu_{\text{prep}} = 1.44 \times 10^{-4}$ and $\Lambda_{\text{prep}} = -2.5 \times 10^{-5}$ for the magic state preparation model Eq. (20). Finally, the parity-check time was set to W = 450 nanoseconds. All experiments were conducted with $\alpha = 0.1$, as preliminary results showed that variations in α had minimal impact on the solution to the problem.



FIG. 6: Space and time cost estimates for a circuit with $T = 10^6$ and $Q = 10^3$ and computers with $\Lambda_{\text{mem}} = 10$. The Pareto front points are highlighted, indicating the optimal solutions for the architecture design problem. The point where $\beta = 1$ represents the serial scheduling case. The points to the left of $\beta = 1$ assume different degrees of circuit parallelization, while those to the right reflect increasing β values until all distillation levels have only one unit.

A. Space and Time Cost Estimates

Figure 6 presents the space and time cost estimates for a quantum circuit with one billion non-Clifford gates and 1000 logical data qubits. Each point in the figure represents a solution to the architecture design problem for a predefined value of β , ranging from $\beta = 0.2$ to the case where each distillation level has only one unit. The Pareto frontier is highlighted, showing the optimal trade-offs between space and time costs. The solutions on this frontier range from 1.9 seconds and 4.5 million physical qubits (for $\beta = 0.2$) to 1.7 minutes and 2.7 million physical qubits (for $\beta \approx 10$).

In the best-case time scenario, assuming a highly parallelizable circuit (for $T_{\text{depth}} = 0.2T$), a 5× speedup could be achieved with 50% more qubits compared to serial execution (for $\beta = 1$). The trend in the plot demonstrates that physical qubit counts increase rapidly as runtime is further reduced, indicating how costly it is to implement the extra resources needed in an MSF to produce magic states sufficiently quickly to allow performing operations in the core processor in parallel whenever possible.

Looking in the other direction, the space-optimal solution reduces the number of physical qubits by 11% compared to serial scheduling, and it slows down execution by a factor of $10\times$. Both solutions require two distillation levels (i.e., L = 2), but, for $\beta = 1$, the number of distillation units is $u \in \{56, 9\}$, whereas for $\beta = 10$, it is reduced to $u \in \{6, 1\}$. This represents a significant reduction in MSF size—from around 386,000 to 39,000 physical qubits—given the code distances $d \in \{7, 17\}$. The two spikes observed for the physical qubit estimates in the plot of Fig. 6 reflect increases of d_{L+1} from 23 to 25 and then to 27.

B. Circuit Parameter Sensitivity

To illustrate how different circuits' characteristics affect resource estimates, Fig. 1a presents space and time cost estimates for varying circuit sizes in the ranges $T \in \{10^6, 10^9, 10^{12}, 10^{15}\}$ and $Q \in \{10^2, 10^3, 10^4\}$. These magnitudes are applicable to a broad spectrum of quantum applications. Only the Pareto frontier points are shown for each circuit size.

For every 1000-fold increase in the value of T, the runtime for the case where $\beta = 1$ increases by a factor of approximately 1000. One important observation is that few space-optimal solutions exist below the serial scheduling case when $Q = 10^4$. This is because, in large core processors, increasing the core processor's code distance makes the overall space costs worse than does saving space by having a smaller MSF. However, in smaller core processors (for $Q = 10^2$), there are opportunities to reduce space costs by downsizing the MSF. In such cases, space can be saved by up to an order of magnitude, while larger core sizes barely affect space costs.

Interestingly, when analyzing circuits of different sizes, we observe that the space requirements for running relatively smaller or larger circuits are comparable. For example, for $Q = 10^2$, the space cost for $T = 10^6$ ranges between 10^5 and 10^6 physical qubits, while for $T = 10^{15}$, the space requirements increase by less than an order of magnitude. In the cases where serial scheduling is employed, physical space requirements increase from approximately 7×10^5 to 2×10^6 qubits.

C. Hardware Noise Parameter Sensitivity

Next, we performed experiments to analyze the sensitivity of space and time estimates to changes in the hardware noise profile, particularly, by varying the error suppression factor Λ_{mem} and magic state preparation error rate e_{prep} . Figure 1b shows the results for a circuit with $T = 10^{12}$ and Q = 100, considering the combinations of $\Lambda_{\text{mem}} \in \{3, 5, 10\}$ and preset values of the magic state preparation error rates $e_{\text{prep}} \in \{10^{-2}, 10^{-5}, 10^{-8}\}$.

The figure shows that, under a scenario where the circuit has a parallelization potential leading to a $5\times$ speedup compared to the serial case, the circuit could be run in 1–2 months depending on the quality of the physical qubits and the prepared magic states. The primary bottleneck in terms of time is the increased code distance in the core processor due to lower-quality qubits. For example, the worst-case scenario requires a 2.5 times higher encoding for the core processor than the best-case scenario. This difference also affects space requirements—5–10 times fewer physical qubits are needed in the case where the error suppression factor and magic state preparation error rate are of their best values as compared to the worst.

This analysis also shows the trade-offs between improving magic state preparation error rates and enhancing the error suppression factor. For instance, with a one-year runtime budget, improving magic state preparation reduces the physical qubit requirement from 2×10^7 to 1×10^7 , while improving the suppression factor yields a greater reduction, that is, to 1×10^6 for the scenarios tested.

VI. CONCLUSION

In this paper, we have presented a method for designing a fault-tolerant quantum architecture that optimizes the trade-offs between the space and time costs needed to execute large-scale quantum circuits. Our approach integrates a core processor designed for efficient logical qubit operations with a multi-level magic state factory that supplies high-fidelity magic states, enabling an effective implementation of non-Clifford gates, which is required for universal quantum computation. We developed a fast heuristic algorithm to optimize the architecture under different FTQC protocols and circuit and hardware parameter settings, providing a flexible framework for estimating quantum resource requirements.

The main takeaway from our experiments is that quantum resource estimates can be quickly generated when a few key parameters are known, such as the circuit volume (in terms of $\pi/8$ rotation gates and logical qubits requested), the error suppression rates of the quantum error correction scheme, and the specific protocols used for magic state preparation, growth, and distillation. Although certain simplifying assumptions were made to facilitate model development, such as using the same distillation protocols across all distillation levels, the proposed framework is adaptable to other quantum architectures, including alternative MSF designs and other resource state factories.

We observed that, depending on the circuit and hardware characteristics, the quantum error correction scheme in the proposed architecture requires between 100,000 and 100 million physical qubits. Lower qubit counts (as low as 10,000) are achievable in scenarios with near-perfect magic state preparation or very high quality QPUs. However, decade-long execution times are still prohibitive for utility-era quantum computers. To mitigate this issue, future research should focus on discovering novel quantum algorithms, improving circuit synthesis and compilation, and drastically improving hardware quality.

Several avenues for future work have arisen from this study. First, improved FTQC protocols can change the resulting resource estimates, which may affect some of the conclusions we have drawn. Additionally, our concept architecture in this paper has a free-space layout, but constraints such as the size of individual QPUs and quantum interconnects between multiple QPUs for distributed quantum computing can be incorporated. Finally, our approach can be applied to design other resource factory modules beyond the $|T\rangle$ states, such as Toffoli states, QROMs, and resource states for specific rotation angles, further broadening the applicability of our approach to quantum architecture design.

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| Variable/Parameter | Description |
|---|--|
| Quantum Circuit | |
| Т | Number of $\pi/8$ rotations in the circuit |
| $T_{ m depth}$ | Circuit depth |
| t_i | Number of $\pi/8$ rotations at each depth $i \in \{1, \ldots, T_{depth}\}$ |
| Q | Number of logical qubits in the circuit |
| q_i | Number of logical qubits requested by each $\pi/8$ rotation $i \in \{1, \ldots, T\}$ |
| Compilation | |
| $V_{ m idle}$ | Idling volume |
| $V_{ m act}$ | Active volume |
| C_{L+1} | Magic state consumption rate in the core processor |
| C_ℓ | Magic state consumption rate at the level ℓ of the MSF |
| D_ℓ | Magic state production rate at the level ℓ of the MSF |
| D_0 | Magic state production rate at the preparation area |
| FTQC Emulation | |
| W | Parity-check time |
| $\mu_{ m mem}, \Lambda_{ m mem}$ | Quantum memory error prefactor and error suppression rate |
| $\mu_{ m prep}, \Lambda_{ m prep}$ | Magic state preparation error prefactor and error suppression rate |
| Magic State Distillati | on |
| M | Number of magic states required per distillation cycle |
| N | Number of magic states distilled per distillation cycle |
| 0 | Number of logical cycles in a distillation cycle |
| Р | Acceptance probability of the protocol |
| Error Rates | |
| E | Error budget |
| $E_{ m msf}$ | Magic state factory errors |
| $E_{ m core}$ | Core processor errors |
| $e_{ m surg}$ | Lattice surgery error rate |
| $e_{ m cliff}$ | Average logical Clifford operation error rate |
| $e_{\mathrm{mem},\ell}$ | Logical quantum memory error rate for qubits at the level ℓ (MSF + core) |
| $e_{ m msf}$ | Magic state error rate output from the MSF |
| $e_{\mathrm{in},\ell}, e_{\mathrm{out},\ell}$ | Magic state error rate input to the level ℓ (MSF + core) and output from the level ℓ (MSF) |
| $e_{\mathrm{grow},\ell}$ | Magic state error rate after growth at the level ℓ (MSF) |
| $e_{ m prep}$ | Magic state error rate after preparation |
| Costs | |
| R | Total expected runtime (time cost) |
| S | Total number of physical qubits (space cost) |
| Decision Variables | |
| α | Average lattice surgery size relative to the number of logical qubits in the core processor |
| eta | Target slowdown factor |
| L | Number of distillation levels |
| K | Total number of logical cycles required to execute the algorithm (makespan) |
| d_ℓ | Code distance for all logical qubits at the level ℓ (MSF + core) |
| u_ℓ | Number of distillation units used at the level ℓ (MSF) |
| | |

APPENDIX A: Overview of Variables and Parameters