RSFQ All-Digital Programmable Multi-Tone Generator For Quantum Applications

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Abstract—One of the most important and topical challenges of quantum circuits is their scalability. RSFQ technology is at the forefront of replacing current standard CMOS-based control architectures for a number of applications, including quantum computing and quantum sensor arrays. By condensing the control and readout to SFQ-based on-chip devices that are directly connected to the quantum systems, it is possible to minimise the total system overhead, improving scalability and integration. In this work, we present a novel RSFQ device that generates multi tone digital signals, based on complex pulse train sequences using a Circular Shift Register (CSR) and a comb filter stage. We show that the frequency spectrum of the pulse trains is dependent on a preloaded pattern on the CSR, as well as on the delay line of the comb filter stage. By carefully selecting both the pattern and delay, the desired tones can be isolated and amplified as required. Finally, we propose some architectures where this device can be implemented to control and readout arrays of quantum devices, such as qubits and single photon detectors.

I. INTRODUCTION

Rapid Single Flux Quantum (RSFQ) [\[1\]](#page-8-0), [\[2\]](#page-8-1) electronics and their energy efficient version (ERSFQ) [\[3\]](#page-8-2), [\[4\]](#page-8-3) are well developed technologies that are now being considered and implemented for the control and readout of quantum circuits such as qubits $[5]-[9]$ $[5]-[9]$ $[5]-[9]$, and quantum sensors $[10]-[12]$ $[10]-[12]$ $[10]-[12]$. As a result, many of the bulky standard room temperature electronics are being replaced by RSFQ circuits that can perform the same quantum circuit manipulation, but with potentially better scalability from decreased system overheads, better integration for cryogenic temperatures due to the much lower power dissipation, and faster operation (up to hundreds of GHz [\[13\]](#page-8-8)). Naturally, this leads to proposed architectures where a full manipulation of qubits and single photon detectors, such as Superconducting Nanowire Single Photon Detectors (SNSPDs), is done in a fully digital and, therefore, more scalable way [\[14\]](#page-8-9).

One circuit of interest in this area is an arbitrary waveform generator (AWG), which at its core consists of a Digital-to-Analogue Converter (DAC), that can generate programmable arbitrary analogue signals. This is the quintessential device used in a myriad of control protocols, including standard microwave based single qubit gates [\[15\]](#page-8-10) or time-domain measurements of RF-SNSPDs [\[16\]](#page-8-11). In particular, AWGs are able, and widely used, to generate multi-tone signals for use in frequency division multiplexing (FDM) control architectures [\[17\]](#page-8-12), [\[18\]](#page-8-13). The RSFQ implementation of such a device usually consists of a digital pulse-based stage which encodes the analogue signal into a binary code that is then followed by a DAC stage, using voltage multipliers or SQUID stacks $[19]-[22]$ $[19]-[22]$ $[19]-[22]$. The only demonstration of multi-tone signal generation using SFQ-based circuits has been recently achieved for metrology applications using the same architecture type mentioned before, with a DAC at the output $[21]$. Here we present an alternative way of generating programmable multitone signals with all-digital pulse based signals, which we name Digital Multi-Tone Generator (DMTG).

Like the previously mentioned implementations of AWGtype RSFQ circuits, Circular Shift Registers (CSR) [\[23\]](#page-9-0)–[\[26\]](#page-9-1) are at the core of this work too, since they can be used as pulse train generators and the type of pulse train is dependent on the initial pre-loaded data on the memory cells of the CSR. This property allows the creation of evenly and unevenly spaced patterns that can be controlled to generate the desired tones on the output signal. This is also an important property when trying to encode an analogue signal into a digital pulse train. The second important component is a Comb Filtering stage [\[27\]](#page-9-2) like those seen in Cascaded-Integrator-Comb filters, both in classical and RSFQ applications, used for decimation and interpolation filter devices [\[28\]](#page-9-3), [\[29\]](#page-9-4). This component is also seen in some pulse multiplier circuits [\[19\]](#page-8-14). In this work, comb filters are implemented to redistribute the power of the CSR output to frequencies that depend on the characteristics of the delay path. This improves the power of the desired tones and attenuates spurious tones if correctly tuned. A feedforward implementation is chosen to comply with RSFQ device restrictions, such as summation and multiplication of single SFQ pulses.

The remainder of this paper is organised as follows. Section [II](#page-1-0) explains the mathematics of pulse trains and their frequency spectra, and how the use of CSR can modify them in a programmable way. Here an analysis of comb filters is also shown, as a way to improve the final spectrum of the signal. Section [III](#page-3-0) then presents the proposed implementation using RSFQ basic components, with special emphasis on the CSR, the clocking network, and the comb filter stage. Section [IV](#page-5-0) shows the simulated results of a 8-bit DMTG using a superconductor circuit simulator, as well as a study of how SFQ pulse characteristics influence the final spectrum. In

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Fig. 1: Example of pulse trains generated in an 8-bit CSR, with programmability focused on tones below $f_{\text{clk}} = 10 \text{GHz}$: (a) Evenly spaced pulse train generates an evenly spaced frequency spectrum (frequency division patterns). (b) Uneven spaced pulse train generates a richer spectrum with more tones. Pattern '1001 1001' generates tones at 2.5 and 7.5 GHz. All spectra from the CSR are periodic with period equal to f_{clk} . (c) Single stage comb filter applied on same pattern as (b), with delay τ = 0.33 ns, tunes the spectrum in a way to amplify the 2.5 GHz tone and cut off the 7.5 GHz tone. FT is normalised for the maximum power in each system, which corresponds to the pattern '1111 1111'. FT scale different between plots for visualisation purposes.

Section [V,](#page-6-0) some applications envisioned for this device are presented. Finally conclusions are given in Section [VI.](#page-7-0)

II. MULTI-TONE DIGITAL SIGNALS WITH PULSE TRAINS

Before introducing SFQ pulses in this work, this section will be concerned with the creation of multi-tone signals using ideal pulse trains. Later, we shall see that this approximation holds extremely well when dealing with SFQ pulses due to their sub picosecond time width.

A. Spectral Analysis

To start this analysis, we assume that a single SFQ pulse is modelled by an infinitely narrow pulse which takes the form of a Dirac delta function:

$$
\delta(x) = \begin{cases} +\infty, & x = 0 \\ 0, & x \neq 0 \end{cases}
$$
 (1)

A pulse train, like one generated by a simple SFQ-DC driver circuit clocked at a certain frequency f_{clk} , can also be written using Dirac functions, by infinitely summing them:

$$
III_T(x) = \sum_{m = -\infty}^{+\infty} \delta(x - mT)
$$
 (2)

where $T = 1/f_{\text{clk}}$ and III represents the Dirac Comb function. These equally spaced pulse trains (with period T), have a Fourier Transform (FT) given by:

$$
\mathcal{F}[\amalg \mathcal{F}[\amalg \mathcal{F}](f)] = \int_{-\infty}^{+\infty} \amalg \mathcal{F}(x) e^{-2\pi j f x} dx = \frac{1}{T} \amalg \mathcal{F}(\mathcal{F}) \quad (3)
$$

This result shows that the frequency spectrum of an ideal and equally spaced pulse train, is itself an equally spaced pulse train with 'period' given by $1/T$, as shown in Fig. $1(a)$. With these types of pulse trains, it is already possible to generate a multi-tone signal, composed of f_{clk} and its harmonics, but the only way to control these tones is to change the frequency of the drive signal, which modifies all the tones in the signal.

Using a CSR, we can redefine the Dirac Comb function to include the pattern loaded in this circuit:

$$
\tilde{\mathrm{L}}\tilde{\mathrm{L}}_{\mathrm{T}}^{\mathrm{N}}(x) = \sum_{m=-\infty}^{+\infty} \sum_{k=0}^{\mathrm{N}-1} S_k \delta(x - k\mathrm{T} - m\mathrm{N}\mathrm{T}) \tag{4}
$$

where the CSR is driven by a clock frequency $f_{\text{clk}} = 1/T$, N is the number of bits of the CSR, and $S_k = \{0, 1\}$ represents the bit (pattern) stored inside memory cell k of the CSR. The frequency spectrum of these unequally spaced pulse trains can be calculated in the same way and it is given by:

$$
\mathcal{F}[\tilde{\mathbf{H}}_{\mathrm{T}}^{\mathrm{N}}(x)](f) = \frac{1}{\mathrm{NT}} \mathbf{H}_{\frac{1}{\mathrm{NT}}}(f) \cdot c(f) \tag{5}
$$

where $c(f)$ is a modulation function given by the pattern in the CSR:

$$
c(f) = \sum_{k=0}^{N-1} S_k e^{-2\pi j f kT}
$$
 (6)

This shows that the result of the CSR is to modulate a frequency pulse train with spacing equal to f_{clk}/N (III $_{\frac{1}{N_T}}$), depending on the pattern loaded on it (S_k) . Using Euler's formula, the modulation function can be interpreted as a summation of sine waves, similar in concept to a Fourier Series, but limited in number and amplitudes. An example

of this modulation is shown in Fig. $1(b)$, with a pattern of '1001 1001', for a 8-bit CSR clocked at 10 GHz. With this, the tones at 2.5 and 7.5 GHz are generated at equal power, while keeping the clock frequency the same. The same tones are generated at $\{2.5, 7.5\} + n.10$ GHz, since the FT keeps its periodicity of f_{clk} .

An important characteristic of the patterns and spectra generated by a CSR is the uniqueness of each one of them. We define a unique pattern for an N-bit CSR as a pattern that generates a frequency spectrum with a unique combination of tones, and a unique combination of relative powers between them, that no other pattern with the same bit length can generate.

The total amount of possible patterns for an N-bit CSR is given by $2^N - 1$. Since most of these are not unique, we define some rules to obtain a minimal set of patterns that can generate all others. To help us study the uniqueness of patterns, some definitions are useful: first, for a N-bit pattern, we define S as the number of set bits, that is, the number of 'ones' in the pattern. Secondly, we define a distance variable D as a set of distances (cyclical) between all set bits in the pattern, where we define a distance of 1 for two consecutive set bits. This set has a cardinality equal to S and the sum of its values must equal the total number of bits N for a valid pattern. For instance, the pattern '1001 1001' for an 8-bit CSR (see Fig. $1(b)$, has a number of set bits $S = 4$ and the distance set is $\mathcal{D} = \{3, 1, 3, 1\}.$

The first rule that stands out to eliminate duplicate patterns is that any pattern with the same number of set bits S and the same distance set D generates the same pattern. For instance, patterns '1000 0000' and '0100 0000' both have $S = 1$ and $D = \{8\}$. This type of bit shift results in a phase shift of the pulse train, but has no effect on the tones generated. This rule can be extended to include patterns whose distance set is a cyclic permutation (CP) of another (e.g. $\{1, 3, 1, 3\}$ which is obtained by shifting $\{3, 1, 3, 1\}$.

Secondly, infinitely long pulse trains exhibit time-reversal symmetry, meaning their spectra remain unchanged whether the pulse train is run from $t_0 \rightarrow t_1$ or from $t_1 \rightarrow t_0$, where $t_1 > t_0$. This means that within a set of noncyclical permutations (NCPs), we can remove further potential duplicate patterns by performing a 'mirror' operation. For instance, taking a few periods of the pattern '1101 0000' with $D = \{1, 2, 5\}$, and running it backwards (-t), it is possible to observe that the pattern '1100 0010' with $\mathcal{D} = \{1, 5, 2\}$ is obtained, both generating the same frequency spectrum, as confirmed through later simulations.

Heuristically, there is another rule that removes additional patterns from the unique set, despite not following completely our original definition of uniqueness. For each pattern obtained so far, there exists a pattern (defined as its dual) obtained by performing a bitwise NOT operation, that also generates the same tones, with the same power relative to each other, except the tones generated at $\{n \cdot f_{\text{clk}}\}$ which have greater or lower power output depending on how many bits are set in the pattern. From the definition, we count every dual pattern as a unique pattern since the output power of these tones have a higher power than the original pattern, although the

remaining tones powers are equal. For instance, the patterns '1000 0000' $(S = 1, \mathcal{D} = \{8\})$ and '0111 1111' $(S = 7, \mathcal{D} = \{8\})$ $\overline{\mathcal{D}} = \{1, 1, 1, 1, 1, 1, 2\}$ generate exactly the same tones, except the tones at $\{n \cdot f_{\text{clk}}\}$ which have increased power for the latter (more sets bits correspond to higher total power at the output). By definition, every pair of dual patterns must have a sum of their set bits equal to N.

With these dual patterns, one can obtain a smaller set of unique patterns below f_{clk} , since one needs only to look at unique patterns with set bits $S = \{1, 2, \ldots, N/2\}$. These are shown for an 8-bit CSR in Fig. [2,](#page-2-0) clocked at 10 GHz. The higher the number of set bits in the pattern, the higher the power spectral density. In a similar way, the more tones spread through the spectrum, the lower the spectral density for each one. This is easily seen with patterns '1000 0000' and '1111 1111', where the former has S=1 and all f_{clk}/N tones with their amplitude reduced by two orders of magnitude, when compared to the latter, with S=8 and only one tone.

Fig. 2: Unique Patterns for an 8-bit CSR clocked at $f_{\text{clk}} = 10$ GHz. Uniqueness of each pattern defined by which tones it generates and the relative power between all of them. Bold patterns correspond to frequency division patterns (equally spaced in time and frequency). For each pattern shown (with exception of '1111 1111'), there exists a dual pattern that generates the same tone distribution but with the tone at $f_{\rm clk}$ having increased power. Width of tones is artificially increased for visualisation purposes, since we are using Dirac delta functions. FT is normalised to the maximum output power of the system, corresponding to the pattern '1111 1111'.

These rules allow us to create a procedure to generate the unique patterns for any N-bit CSR, as shown in Algorithm [1.](#page-3-1) This procedure grows exponentially with the number of bits, since it requires various calculations of combinations and permutations. As expected, the number of unique patterns grows in a similar way, although slower than the original 2^N . Two boundaries can be defined for a quick estimation of this number: the lower boundary is defined as the sum of all scombinations of the set $S = \{1, 2, \ldots, N\}$ whose sum of elements equal N. The higher boundary is obtained from the latter, by adding the unique non-cyclic permutations (NCP) for each combination. The real number is then obtained by using procedure [1](#page-3-1) and dual patterns to eliminate some of the extra NCPs from the higher boundary that generate equal spectra.

Increasing the number of bits, N, in the shift register increases the frequency resolution since the base pulse train in the frequency space, defined in Eq. [\(5\)](#page-1-2), is equally spaced by $1/NT = f_{\text{clk}}/N$. This means more tones can be generated within the same frequency range from 0 to f_{clk} . Another additional benefit of increasing the number of bits, is that for a long enough CSR, it is possible to simply overlap evenly spaced pulse trains of different frequencies and obtain a pattern with these frequencies only.

B. Comb Filtering

Using a CSR with a pre loaded pattern increases the control of the tones generated with pulse trains. We can further improve it by using comb filtering stages as shown in this section. There are two types of comb filters: feedback and feedforward filters [\[27\]](#page-9-2). These can be defined as two-port circuits, where a delayed version of the output or input signal (respectively) is added onto itself. Mathematically:

$$
y(t) = x(t) + \alpha y(t - \tau), \text{ [Feedback]} \tag{7}
$$

$$
y(t) = x(t) + \alpha x(t - \tau), \text{ [Feedforward]} \tag{8}
$$

where $x(t)$ is the input signal, $y(t)$ is the output signal, τ is the added delay and α is the scaling factor of the delayed signal. A block diagram of both types of filters is shown in Fig. [4\(b\).](#page-4-0) While the latter type has a potentially better amplitude response (specifically, it can target some tones more effectively due to the sharper frequency spectrum), its implementation using RSFQ circuits is not as straightforward, since the scaling factor needs be less than 1 to avoid instabilities in the filter output. To have the scaling factor less than 1, the top branch of the comb filter would need to have Josephson junctions with I_cR_N product different from the rest of the circuit. Therefore, and as a first proof of concept, we look at the feedforward implementation and how it is used in the DMTG.

Taking the Fourier Transform of Eq. (8) , we obtain:

$$
\mathcal{F}[y(t)](f) = \mathcal{F}[x(t)](f) + \alpha \mathcal{F}[x(t-\tau)](f)
$$

= $(1 + \alpha e^{-2\pi j f \tau}) \mathcal{F}[x(t)](f)$ (9)

Like the previous section with the CSR pattern, this result shows that the modulation is achieved by summation of sine waves, but in this case, their frequency can be fine tuned by the delay of each filtering stage. There is, however, an exception to the usefulness of the comb filter, which happens when the delay matches the period spacing of the clock $(1/f_{\text{clk}})$. When such circumstances occur and because SFQ pulses cannot be added together (as in, on the same time instance, two pulses will not sum their amplitudes), the comb filter either produces no delayed pulse, so the spectrum will be exactly the same as it is seen at the end of the CSR, or it produces a delayed pulse which effectively changes the original pattern of the CSR into another pattern.

Fig. [3](#page-4-1) shows an example of the effect of using a feedforward comb filter stage on a 8-bit CSR with a preloaded pattern of '1001 1001'. As the delay is tuned from 0 to N/f_{clk} , the tones at 2.5, 7.5 and 10 GHz are periodically tuned from 0 to a maximum amplitude. A cross section of the 2D plot can also be seen, where the periodic behaviour of the tones at 2.5 and 7.5 GHz is plotted, together with a curve showing the distance between these two tones. By selecting the correct delay, we can tune both tones to be at a maximum of separation (for example to suppress the 7.5 GHz tone, with delay 0.33ns) or a minimum of separation, which for this pattern corresponds to both tones at equal strength. Fig. $1(c)$ shows the result of selecting a delay equal to 0.33 ns on the output of the CSR. As predicted, the tone at 7.5 GHz is suppressed.

III. RSFQ IMPLEMENTATION

A. Circular Shift Registers

CSRs are an extension of linear shift registers, where the output of the last memory cell is connected to the input of the first, creating a circular flow of data (Fig. $4(a)$). An N-bit CSR consists of N D Flip-Flops (DFFs) connected in series using Josephson Transmission Lines (JTLs), to control the delay between cells. To clock the CSR, 2-way splitters are usually used, however, in this device we use 3-way splitters to meet the requirements of our clocking network, as will be explained below.

Shift registers are synchronous circuits, meaning they require a clock to advance to the next internal state, independent of the data inputs. The type and architecture of the clock distribution network is therefore crucial for the correct operation of this device, considering all internal and external delays on the data and clock paths. Particularly important is the clock skew, t_{cs} , of the circuit, which for a CSR must equal to 0 [\[24\]](#page-9-5), [\[30\]](#page-9-6). This quantity is defined as the time between a clock pulse arriving at the ith memory cell and the same clock pulse reaching the $(i + 1)$ th cell (see Fig. [4\(a\)\)](#page-4-0). For a CSR:

$$
t_{\rm cs}^{\rm Total} = \sum_{i=1}^{N} t_{\rm cs}^i = (t_1 - t_2) + (t_2 - t_3) + \ldots + (t_N - t_1) = 0
$$
\n(10)

Fig. 3: Comb filter effect on frequency spectrum for the same pattern and CSR shown in Fig. [1](#page-1-1) (b). (a) 2D view of spectrum versus comb filter delay. (b) Slice view of the two frequencies of interest (2.5 and 7.5 GHz) and a curve (green) illustrating the difference between these two latter, which is utilised to adjust the two tones in relation to each other. In this example, the largest difference is achieved for a delay ~ 0.066 ns, or 0.333 ns, where the amplitude of the 7.5 GHz tone is reduced to zero; or 0.133 and 0.266 ns, where the latter tone is amplified and the 2.5 GHz tone reduced, but not removed.

where $t_{\text{cs}}^i = (t_i - t_{i+1})$, and t_i is the time when clock pulse arrives at the ith cell. To avoid any racing conditions, the clock skew for each cell plus the data delay between cells must be greater than the hold time of the cell. This must still be met, even though the total clock skew of the CSR is zero.

To satisfy this condition, a type of clocking network was designed which is based on a type of symmetrical-mixed clock design as seen in Refs. $[22]$, $[24]$, $[26]$. Here, N/2 bits of the shift register are clocked in a concurrent way and the remaining N/2 bits are clocked in a counter flow manner, but only one input and output of data are used, as shown

Fig. 4: (a) Diagram of N-bit linear shift register being clocked in a concurrent or counter flow. t_n represents the time when the clock signal arrives at memory cell n. The total clock skew of a circular shift register (dotted) is equal to zero. (b) Diagram of two types of comb filters: feedback [left] and feedforward [right], both with a delay and scaling factor stage. (c) Block diagram of a DMTG, using a N-bit CSR and a single stage comb filter step. Full symmetric clock distribution is used with N/2 bits having concurrent flow and the remaining N/2 having counter flow of data and clock. A non destructive readout cell (NDRO) is used to ensure a way of writing data in the CSR and forming the loop to generate the pulse train, as well as used in the comb filter to allow a zero delay output (Set and Reset). D-JTL (delay JTL) is used as a tuneable way of changing the fluxon propagation speed in the JTL.

in Fig. $4(c)$. This ensures that the two blocks have negative and positive clock skews, respectively, but when combined in a loop the total equals to zero. Another alternative is to use a standard binary tree clock distribution, which has a higher overhead of splitters. For binary-tree clocking, the clock skew between adjacent memory cells is zero, so the sum will always also be zero. The total amount of splitters necessary for this type of clock network is $N - 1$, whereas for the symmetrical type it requires N/2.

B. Comb Filtering

Comb filtering in RSFQ circuits must be modified slightly compared to the standard digital signal processing filter, since SFQ pulses cannot be summed in amplitude like normal signals can. This means that the two signals generated must be merged, instead of summed. Also, the scaling factor seen in Eq. [\(8\)](#page-3-2) is harder to achieve, specifically when $\alpha < 1$, since the amplitudes of SFQ pulses are set during the design phase by the critical current density j_c and I_cR_N product of the junctions. It is also possible to use an amplifying JTL to increase the voltage of the SFQ pulse and obtain $\alpha > 1$, which can be useful for increasing the power of the output tones.

The implementation of comb filtering in this work is based on the feedforward architecture with a unity scaling factor. The circuit has three basic RSFQ cells: one splitter to generate the two data paths, one merger to combine the two pulses and one long JTL, which we call a delay JTL, which delays the propagation of SFQ pulses in one branch of the circuit. This delay (τ) is tuneable by changing the bias current of the entire delay JTL, based on fluxon propagation and interaction in JTLs [\[31\]](#page-9-7). This implementation is shown in Fig. $4(c)$, alongside a full block diagram of the multi-tone generator device, comprised of a N-bit CSR and a single stage feedforward comb filtering stage, with one data input and one data output. A NDRO cell is used to break the loop of the CSR and choose whether the CSR is in write (SET=0) or read mode (SET=1), which opens and closes the loop, respectively. Another NDRO switch is added to the comb filter to allow for an output with no delayed pulse. Alternatively, an RSFQ DC switch could be used as a replacement for NDRO cells, to reduce the complexity and overhead of the design.

IV. SIMULATIONS

To test the operation of the device, a simulation model was implemented using PSCAN2 superconductor circuit simulator [\[32\]](#page-9-8). A netlist of the device was designed using SeeQC's high density fabrication process parameters, specifically devised for digital circuits and quantum applications [\[33\]](#page-9-9). A modular approach is used to optimise the design, starting with the memory cells and the shift register and further adding the comb filter stage. The optimisation process was done at 10GHz (a conventional operation frequency for superconducting quantum circuits), therefore for higher frequencies the margins are expected to be narrower. The global margins XI, XJ, and XL, represent the total deviations of the bias currents, junction critical currents, and inductances, respectively, in the device, such that the correct operation is not compromised. Maximum margins are capped at 40%. These are obtained from the full circuits and tested at different clock frequencies (namely, 10,

| Pattern '1000 1000' | | | Pattern '1001 1001' | | |
|---------------------|--|--|---------------------|--|--|
| | | 10 GHz 20 GHz 50 GHz* | | | 10 GHz 20 GHz 50 GHz^* |
| | | $XI \begin{bmatrix} -28,25 \end{bmatrix}$ $[-21,25]$ $[-21,18] \begin{bmatrix} -28,25 \end{bmatrix}$ $[-22,23]$ $[-21,18]$ | | | |
| | | XJ [-22,25] [-22,18] [-16,23] [-20,25] [-19,18] [-16,18] XL [-40,40] [-40,40] [-40,40] [-40,40] [-40,40] [-35,34] | | | |
| | | | | | |

TABLE I: Simulated Global Margins for an 8-bit device (in percentages).

20 and 50 GHz) and with different patterns on the CSR. For operation around 50 GHz and above, slight modifications of the CSR were made, increasing the I_cR_N product for faster practical circuit operation and removing some JTLs between data cells. A maximum frequency of 86 GHz was obtained with correct operation of the CSR without the comb filter, as a demonstration of the robustness of the design. A summary of these tests is shown in Table [I.](#page-5-1)

The output frequency spectrum was obtained from the simulations by using the Lomb-Scargle periodogram [\[34\]](#page-9-10). This algorithm provides an estimation of the discrete Fourier Transform for samples with unevenly spaced time data, which is crucial for the analysis of PSCAN2 simulations due to its dynamic time step.

The dependence of the frequency spectrum on the characteristics of the SFQ pulses comprising the pulse train was also investigated and is shown in Fig. [6.](#page-7-1) Firstly, by changing the characteristic voltage V_c of the output junctions, we observe a change in the relative powers between the tones of the signal, as shown in Fig. $6(b)$. This is in agreement with the result obtained in Ref. [\[7\]](#page-8-17), where for narrow pulses, the higher frequency components have increased power. This can become a problem when working with superconducting circuits since at some critical power these high frequency tones may break Cooper pairs and poison the system with quasiparticles [\[8\]](#page-8-18). In practice, the advantage of having narrower pulses is to make the pulse trains and subsequently the control pulses, shorter in time. Since the area of the pulse, Φ_0 , remains the same, the average power output also does not change.

Increasing the pulse train length improves the bandwidth of the output tones, as seen in Fig. $6(c)$. The longer the pulse train, the narrower the tones, which in practice means our control pulse trains cannot be too short in time. The average power output is the same in the time domain (since the peak power and the duty cycle remain constant), although there is more energy in the system.

Clock jitter is another metric which exists in real experiments and can affect the frequency spectrum of the output signal. While the base simulations shown do not include a known and controllable source of jitter, there is a small variation of the clock period due to the way the simulation, particularly the dynamic time step calculation, is performed, but accounts for less than few picoseconds. Adding more jitter, the tones tend to shift from their expected value by a few MHz (as seen on the right side of Fig. $6(b)$, where the tone at 100 GHz slightly shifts) and noise at higher frequencies increases.

When discussing powers with pulse trains and frequency spectra, one must distinguish between a couple of variables.

Fig. 5: Frequency spectra obtained from PSCAN2 time simulations using the Lomb-Scargle periodogram algorithm for a 5 ns pulse train. The same pattern used in Fig. [1\(c\)](#page-1-1) is used for comparison, without (a) and with (b) the comb filtering stage set very close to the 0.333 ns delay to obtain the best separation between the two tones, 2.5 and 7.5 GHz (as shown in Fig. [3\)](#page-4-1). Dashed lines on time domain plots show the input data (pre-loading) sent to the CSR. Insets highlight one SFQ pulse (top), as well as the width of one of the frequency tones (bottom).

The average power in the time domain of a pulse train will be given by:

$$
P_{avg} = P_{peak} \cdot Duty \; Cycle = P_{peak} \cdot \frac{\sigma_{pulse}}{T_{clk}} \cdot \frac{n}{N} \qquad (11)
$$

where $T_{\text{clk}} = 1/f_{\text{clk}}$, σ_{pulse} is the width of each SFQ pulse and n is the number of set bits in an N-bit pattern. Increasing the pulse length, as done in this work, increases the total energy in the signal, but the average power in time domain remains. For the Lomb Scargle periodogram algorithm, the result is a metric of the squared amplitudes of each Fourier component at each frequency, with units of mV^2 in this work. This is known as the Power Spectrum (PS). Since we are dealing with discrete signals, that is, sampling rate and number of points are finite, one drawback is that the DFT and all estimations scale with the number of points N of our original signal, making the amplitude of the calculation arbitrary and with no real meaning. For the transform to be useful, we calculate the Power Spectral Density (PSD) which is obtained by dividing the power spectrum by the frequency resolution of the spectrum:

$$
PSD \equiv \frac{PS}{f_s N} \tag{12}
$$

where f_s is the frequency resolution and N is the number of sample points. Using the PSD, the area under each tone represents the fraction of the signal power that is concentrated around that tone. Increasing the total length of the pulse train therefore decreases the tone width, but amplitude increases so that the total area remains constant, since the input power remains the same (higher length means more energy but averaged over longer period).

V. OUTLOOK

The DMTG device presented and discussed herein has applications in both classical RSFQ circuitry, as well as a control circuit for quantum systems that also require a cryogenic environment and the higher frequencies achieved with RSFQ and ERSFQ technologies. Two examples which motivated this work are qubit and SNSPD control and readout systems.

For standard qubit control, a microwave pulse is carefully crafted to excite single qubit gates and drive qubit state rotation on the XX and YY axes. For this method, our device could be used as a way to multiplex the control and use a single line for many qubits, after it is filtered and impedance matched on a RF module, as shown in Ref. [\[35\]](#page-9-11).

Currently, SFQ-based digital control is achieved using a simple DC-SFQ converter (or a combination of such) and clocked at a subharmonic of the qubit transition frequency [\[8\]](#page-8-18). The idea is that each pulse rotates the qubit state slightly around the XX or YY axis of the Bloch Sphere, and by controlling the number of pulses the desired final state can be obtained. The subhamornic is used to avoid driving the qubit directly, since the SFQ system is capacitively coupled to it. Our device could be used like this in a fully digital way or can be used to implement more complex pulse sequences as shown in Ref. [\[36\]](#page-9-12). These sequences can optimise SFQ-based qubit control by reducing leakage outside the computational space and increasing the fidelity of single qubit gates.

Superconducting Nanowire Single Photon Detectors (SNSPD) are another area where superconductor electronics are foreseen to improve scalability. In particular, large arrays of RF-SNSPDs (SNSPDs integrated in lumped element resonators) can be used in conjunction with RSFQ electronics to create a control and readout system that can scale more efficiently than DC-SNSPDs [\[16\]](#page-8-11). The output signal with (a)

 $\mathbf{V}_c{=}1$

Fig. 6: Influence of pulse train characteristics on frequency spectrum for the same pattern applied to an 8-bit CSR, as seen in Fig. [5,](#page-6-1) focusing on the 2.5 GHz tone. (a) An increasing characteristic voltage, $V_c=I_cR_N$, of the output junctions in the circuit, results in a narrower pulse with an increased amplitude. Difference in time shown corresponds to the small jitter in PSCAN2 simulations. (b) Increasing V_c , the output power of lower frequency tones remains approximately constant, while higher frequencies are amplified. (c) To decrease the width of each tone, a longer pulse train should be considered. For a 50 ns pulse train, a bandwidth of 15 MHz is obtained, compared to 84 MHz for a 5 ns pulse train. V_c is in dimensionless PSCAN2 units, where unity equals 0.287 mV.

multiple tones would be sent to an array of resonators that are coupled to the SNSPDs, and, using frequency multiplexing, all pixels could be probed simultaneously with only one input. The readout architecture would closely follow the same one used for microwave electronics, where a multi-tone input signal is sent to the signal, filtered, and down-converted using IQ mixers, to then be detected by an Analogue-to-Digital Converter, which could also be implemented with RSFQ circuitry [\[37\]](#page-9-13), [\[38\]](#page-9-14). In this case, no down-conversion would be necessary. Additionally, time domain multiplexing could be used to sweep the local oscillator signal (LO) such that the down-converted signal frequency could always fit within the bandwidth of the ADC, reducing the sample rate, but increasing the total bandwidth available for the resonators. The same architecture could be implemented to probe an array of readout resonators coupled to qubits in the standard dispersive regime [\[39\]](#page-9-15). A summary of these architectures is

VI. CONCLUSION

shown in Fig. [7.](#page-8-19)

In conclusion, we have presented a novel RSFQ device that uses the properties of pulse trains and their Fourier Transform, to create multi-tone signals that depend on the data (pattern) loaded in the memory cells of an N-bit CSR. We have shown the existence of and the means to obtain all unique patterns for an N-bit CSR, although the search for optimal and unique patterns is computationally complex and requires exponential time. Together with a feedforward comb filter stage, the tones generated are further concentrated around certain frequencies, which increases the tuneability of the output, as well as increasing the amplitude of the desired tones. Additionally, stacking comb filters can further improve the amplitude and spectrum.

In terms of components, the device is relatively simple to fabricate, uses well developed and studied RSFQ components, and the number of junctions in the circuit grows reasonably well with increasing N. The simulated circuits show a great match with the predicted frequency spectra for every pattern and it is also shown that changing the SFQ pulse width, pulse train length, and clock periodicity has an influence on the result. This is all consistent with the results predicted theoretically. The average margins are shown to be quite good for different patterns at around 20%, which is similar to margins obtained experimentally for RSFQ devices with complexity involving few hundred junctions. It is also shown that the maximum operating frequency is dependent on the characteristic voltage of the junctions, but with this fabrication parameters, operation close to 100 GHz can be achieved.

In the future, a way of improving the algorithm to search for unique patterns with an improved time complexity is required, as well as a method to estimate a set of patterns which can be used, given the tones desired by the user.

ACKNOWLEDGEMENT

This work was funded and supported by the National Manufacturing Institute Scotland and the Scottish Research Partnership in Engineering (SRPe) through the Industrial Doctorate Programme NMIS-IDP/025, SeeQC UK Limited and the University of Glasgow through EPSRC grant no. EP/T025743/1.

Fig. 7: Proposed SFQ-Based Architectures for Qubit and SNSPDs applications utilising the Digital Multi-Tone Generator (DMTG) device presented in this work. (a) Qubit control using a RF module (see Ref. $[35]$) to filter the complex pulse train into an analogue signal to drive XX and YY qubit state rotations. (b) Directly applying the SFQ pulses to the qubit yields a full digital control method, also working as XX and YY qubit gates (see Ref. [\[8\]](#page-8-18), [\[36\]](#page-9-12)). (c) Resonator readout is also possible using a heterodyne scheme where both the multi tone signal and a local oscillator are generated on-chip. Down-conversion can be possibly substituted by a RSFQ based ADC to directly digitise the signal from the quantum system, creating a full RSFQ based control system.

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