LEDRO: <u>LLM-Enhanced</u> <u>Design</u> Space <u>R</u>eduction and <u>Optimization</u> for Analog Circuits

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Abstract—Traditional approaches for designing analog circuits are time-consuming and require significant human expertise. Existing automation efforts using methods like Bayesian Optimization (BO) and Reinforcement Learning (RL) are suboptimal and costly to generalize across different topologies and technology nodes. In our work, we introduce a novel approach, LEDRO, utilizing Large Language Models (LLMs) in conjunction with optimization techniques to iteratively refine the design space for analog circuit sizing. LEDRO is highly generalizable compared to other RL and BO baselines, eliminating the need for design annotation or model training for different topologies or technology nodes. We conduct a comprehensive evaluation of our proposed framework and baseline on 22 different Op-Amp topologies across four FinFET technology nodes. Results demonstrate the superior performance of LEDRO as it outperforms our best baseline by an average of 13% FoM improvement with 2.15× speed-up on low-complexity Op-Amps and 48% FoM improvement with 1.7× speed-up on high-complexity Op-Amps. This highlights LEDRO's effective performance, efficiency, and generalizability.

Index Terms—LLM, optimization, opamp, design, topology, analog, circuit, sizing, FinFET

I. INTRODUCTION

Designing analog circuits involves various subtasks like topology selection, transistor sizing, layout, and verification while optimizing power efficiency, maximizing performance, and reducing the area to meet the target specifications. These subtasks are complex, requiring time-consuming simulations along with human expertise [1]. Minor topological modifications, technology node transfer, and advanced technologies such as FinFETs further increase this human effort. Thus, there is an increasing need to automate the process of analog circuit design.

Recent advancements have introduced automation in operational amplifier (Op-Amp) design by reformulating the sizing and biasing of transistors as an optimization problem [2]. Previous works have explored optimization techniques such as Bayesian Optimization (BO) [2], [3], Reinforcement Learning (RL) [4], [5], and genetic algorithms [6], [7] to solve this problem. However, these approaches treat the circuit design space as a black box, solving without any domain-specific analog design knowledge that an expert analog designer might have, which can lead to sub-optimal solutions. For example, these approaches often overlook the regions of operation or key transistor biasing points. Also, these approaches are costly and not generalizable since they often require retraining for each circuit topology and technology node [4], [5].

Recent works explore utilizing LLMs for analog circuit design [8]-[13], but most of them don't focus on transistor level sizing optimization. Refs. [8], [9] utilize LLMs for analog layout design, [10] uses agentic LLMs to automate design process, and [11], [13] prioritize topology and correct functionality of analog circuits. Ref. [12] focuses on transistor sizing optimization by expecting LLMs to directly provide the optimized sizing value, which can be challenging to scale to larger search spaces. To overcome these shortcomings, we introduce a novel framework - LLM-Enhanced Design Space Reduction and Optimization (LEDRO) - that synergizes the mathematical reasoning from optimization techniques with the circuit knowledge of LLMs. Fundamentally, LEDRO enhances design space exploration by iteratively leveraging LLMs to choose a refined search region (instead of direct points) and optimization techniques to find high-performing circuits in the chosen region. Fig. 1 provides a high-level illustration of LEDRO. To ensure LEDRO's generalizability across technology nodes and topologies, we perform calibration point synthesis using optimization techniques to provide reference examples to the LLM to generate refined regions without requiring any circuit-specific training. To further improve LLM outputs, we provide LLM with its knowledge-based selfreflection and simulation-based optimization feedback. In our work, we utilize LLaMa3-70B [14] as the LLM and TuRBO [15] as the optimization technique for LEDRO.

We compare our framework against a state-of-the-art actorcritic RL framework [4], [16], [17] and a pure TuRBO approach [15]. To benchmark the generalizability of our framework, we evaluate it on one of the most comprehensive setups of 88 different circuits comprising a broad range of 22 Op-Amp topologies across 4 FinFET technology nodes. We divide the topologies into low and high-complexity Op-Amps for finer comparisons. For evaluation, we utilize the Figure of Merit (FoM), an objective function of the normalized, weighted sum of the gain, unity gain bandwidth, phase margin, and supply current. Experiments reveal the broad generalizability of LEDRO with an average FoM improvement of 13% with 2.15× speed-up for the low-complexity Op-Amps over our best baseline and 48% FoM improvement with a $1.7 \times$ speed-up for the high-complexity ones. Thus, we show that



Fig. 1. Illustration of LLM-enhanced design space reduction and optimization (LEDRO).

LEDRO leverages LLMs to refine the search space to more relevant ranges to ensure better and more efficient designs. In addition, LEDRO offers wide versatility as it can be coupled with any optimization method as a plug-and-play approach.

Overall, we summarize our key contributions as follows:

- We introduce a novel framework, LEDRO, which conducts *refined-search space exploration* by combining LLMs with optimization techniques, becoming one of the first works to utilize LLMs for analog circuit sizing.
- We demonstrate the generalizability of our framework on an *extensive experimental setup* comprising 22 Op-Amp topologies across four different technology nodes, particularly in FinFET technology
- We showcase the *superior performance and speed-up* of LEDRO on our benchmarks compared to state-of-theart RL and standalone TuRBO algorithms, establishing LEDRO as a highly effective and efficient framework for analog circuit design.

The rest of this paper is organized as follows. Section II introduces the proposed LEDRO method with a case study example. Section III provides experiment results on a set of diverse circuits and Section IV concludes the paper.

II. METHODS

Our proposed framework LEDRO utilizes a Large Language Model (LLM) in conjunction with an optimization module to more efficiently explore the search space for analog design. A circuit simulator simulates the created analog designs and estimates the performance. LEDRO continually explores and improves the design by running these components in iteration for a fixed set of rounds. In our work, we utilize LLaMa3-70B [14] as the LLM and TuRBO [15] as our optimizer. For LLaMa3-70B, we utilize greedy decoding with temperature of 0.8, and maximum generation length of 1000 tokens. In total, we run LEDRO for ten iterations. We provide a high-level block diagram of LEDRO in Fig 2 and a case study in II-D.

A. Calibration Point Synthesis for LLM

Directly identifying optimal points or regions is a non-trivial task for LLMs since different topologies across technology nodes can have highly diverse optimal points in the complex



Fig. 2. Block-diagram of proposed framework.

design space. Instead, to effectively utilize LLMs, we create a *calibrated initial prompt* which aids the LLM to understand and navigate the search space better. Specifically, we include some reference designs in this prompt that provide this search space calibration and understanding.

To provide these reference designs, we first sample 200 points by running the optimizer over the entire search space as allowed by the technology node. Next, we extract "good" points from these sampled points by filtering the design configurations for which the amplifier gain exceeds a threshold value. We set the threshold to a low 0 dB so that these "good" points are easy to find. In rare cases where no "good" points are found, the optimization can be run longer, or the threshold value can be lowered (although we didn't face such an issue with our experiments). Finally, we rank these filtered "good" points on their Figure of Merit (described in the next paragraph) and add the top five designs to our *calibrated initial prompt* as the reference designs, as shown in Fig 1(A).

Figure of Merit: To quantitatively assess the configurations, similar to [4], [18], [19], we define our Figure of Merit (FoM) by an objective function utilizing the specifications S of gain (G), unity gain bandwidth (f), supply current (I), and phase margin (PM). First we normalize each specification $s \in S$ using its corresponding user-defined boundary value $s_{bound} \in$



Fig. 3. First round prompt and response for folded cascode amplifier.

 S_{bound} by the normalizing function ϕ as

$$\phi(s, s_{bound}) = \frac{s - s_{bound}}{s + s_{bound}}$$

Thus, if $s = s_{bound}$, the normalized value is capped at 0; else $\phi(s, s_{bound}) < 0$. Such capping and normalization ensures the optimization of all specifications rather than the hyper-optimization of a single specification.

We formulate the FoM objective function \mathcal{V} as the weighted sum of the normalized specifications as

$$\mathcal{V}(\mathcal{S}, \mathcal{S}_{bound}; w) = \sum_{(s, s_{bound}) \in (\mathcal{S}, \mathcal{S}_{bound})} w_s.\phi(s, s_{bound})$$

where w_s is the weight assigned for specification s. Owing to the capping in the normalization, the maximum achievable FoM value is 0, with higher FoMs being more desirable.

B. LLM: First Round Prompt

The design search space for amplifiers is high dimensional and complex since each transistor can have a wide array of possible configurations in terms of length, number of fins, and biasing conditions [20]. LEDRO leverages the pre-trained knowledge and reasoning capabilities of LLMs to reduce and refine this design search space, simplifying exploration for subsequent optimizations (as shown in Fig 1(B)). More technically, given the input prompt with the calibration points, LLMs are required to output this refined search space region. **Circuit Representation:** To describe the circuit to LLMs in natural language, we represent it by its netlist. The netlist provides a detailed description of the connectivity and component



Fig. 4. Further feedback and reflection prompts and responses for further rounds for a folded cascode amplifier.

specifications in the circuit. Our studies show that LLMs can parse and interpret the circuit intricacies using the netlist.

Prompt Setup: The LLM prompt comprises the system prompt for high-level instructions and the user prompt for specific inputs and queries. We provide our problem description, which includes the circuit's netlist, amplifier topology, and the specifications in the system prompt. This ensures that these details serve as a continuous reference to the LLM.

For the user prompt for the first round, we provide the problem overview and the design objectives and introduce the initial set of calibrated points (as described in II-A). Each calibrated point is characterized by the specifications (G, PM, etc), the transistor parameters (number of fins, biasing, etc.), the FoM \mathcal{V} , and each transistor's region of operation. We also provide the specification boundary values and the verbalized FoM objective function. Finally, we add instructions prompting the LLM to select and appropriately reduce the design search space, along with output formatting instructions. Detailed information about the transistor operation (cutoff, subthreshold, saturation, or linear region) and its self-knowledge allows the LLM to make informed decisions and efficiently provide the refined search space region. We provide an illustration of this prompt in Fig 3.

LLM to Optimization: The LLM-generated refined search region is then provided back to the optimizer (in our case, TuRBO). We sample 100 points in this reduced space using the optimizer and provide corresponding feedback (discussed in II-C) to the LLM in an iterative fashion. The refined search space from LLMs is the defining feature of LEDRO as it prioritizes regional exploitation by significantly reducing the optimization complexity over a wide-range exploration on the entire search space. This subsequently accelerates the identi-



Fig. 5. Differential folded cascode circuit and gain, UGBW, and FoM for LEDRO with LLaMa3-70b, GPT-3.5-turbo models and BO-1200 vs steps.

fication of high-performing designs and uncovers innovative configurations that might have remained undiscovered with only the optimizer due to higher complexity.

C. LLM: Feedback and Reflection for Further Rounds

For subsequent rounds, we remove the problem description from the LLM prompt and instead add the optimizer feedback and the self-reflection for effective and better-informed search space reduction, as shown in Fig 1(C). The optimizer feedback can be of two forms based on the optimizer's performance within the LLM-provided design space from the last round. If the optimizer performs well - characterized by achieving more than five "good" points along with an increased FoM relative to previous rounds - we provide these new points back to the LLM, acknowledging its effective performance. Contrarily, if the optimizer performs poorly, we provide this feedback to the LLM and ask it to explore a new and different search region.

As part of self-reflection, we prompt the LLM to reflect on its past ranges and strategize what to do next. This selfreflection is inspired by concepts outlined in [21], where we prompt the LLM agent to summarize previous design ranges and look back on its past strategies. Overall, we find that the optimization feedback and self-reflection encourage the LLM to dynamically adjust its exploration strategy and efficiently enhance the refined region. We provide an illustration of the feedback and reflection prompts in Fig 4.

D. Case Study: End-to-end example of 7nm differential folded cascode amplifier

We present a case study for the design of a differentialended folded cascode circuit (as shown in Fig. 5) in 7nm PTM-MG technology [22] using LEDRO. This circuit, chosen for its relevance in past literature [23]–[25], serves as a good benchmark for showcasing our model performance. We conduct calibration point synthesis with TuRBO and add them to the first round prompt for the LLM as shown in Fig 3. For subsequent rounds, we follow up with optimizer feedback and LLM's self-reflection, as shown in Fig 4. We compare the optimization performance of two different runs of LEDRO utilizing two different LLMs with a pure TuRBO optimizer



Fig. 6. Parameters per Op-Amp and division into high and low-complexity Op-Amps and their boundary values.

in terms of Gain, Unity Gain Bandwidth (UGBW), and FoM vs. optimizer steps in Fig 5. As observed, pure TuRBO overoptimizes UGBW and is unable to improve gain over the fixed 1200 iterations. Although TuRBO might be able to reach a similar optimal point, it would take many more optimization steps. On that hand, both runs of LEDRO achieve stronger gain, UGBW, and, in turn, high FoM in fewer optimizer steps. We conduct future comprehensive experiments only using LLaMa3-70B [14] since we validated the utility of GPT-3.5-turbo through this case study and since it is more expensive to run the GPT model.

III. EXPERIMENTS AND RESULTS

We describe our experimental setup in III-A, the main results in III-B and supporting analysis in III-C.

A. Experimental Setup

Benchmarks: To demonstrate the broad generalizability of our framework, we conduct experiments using a diverse set of 22 amplifier topologies, including both PMOS and NMOS input configurations with single-ended and differential-ended output designs. To create this benchmark, we modify and repurpose the subcircuit annotation task in [26] to design the parametrized FinFET netlists. For richer benchmarking, we split the amplifiers into 10 low-complexity and 12 highcomplexity Op-Amps based on the number of optimization parameters. To ensure the robustness of our study, we utilize predictive technology models for multi-gate transistors (PTM-MG) [22] across multiple technology nodes, specifically 7nm, 10nm, 14nm, and 16nm. We show the different Op-Amps along with their categorization and number of parameters in Fig 6.

Evaluation Metric: We consider performance and efficiency as the major evaluation metrics. Following previous works like [12], [19], we utilize the number of optimization steps to measure the efficiency. For performance, the evaluation metric is the Figure of Merit (FoM), as we defined in II-A, using user-defined specification boundary values. Different amplifiers have different characteristics - some achieve higher gain, some are optimized for low power, etc - and thus can



Fig. 7. Performance (FoM) and Efficiency (number of steps) comparison of LEDRO with other baselines for different low-complexity amplifier topologies across four different technology nodes. As shown, LEDRO not only achieves better FOM, but also takes fewer steps to reach the best BO-2000 FoM.

have varied specification boundaries. These characteristics can vary significantly when scaling the same topology across technology nodes. Most previous works [17], [25] experiment with just 1-3 Op-Amps, which allows them to set customized FoM boundary values for each circuit easily. Since our work focuses on a comprehensive benchmark of 22 Op-Amps across four technology nodes, it is challenging and infeasible to set customized boundary values for each circuit.

Instead, we specify two sets of boundary values - one each for the low-complexity and the high-complexity Op-Amp groups. Specifically, for our low-complexity group, we set $G_{bound} = 50 \text{ dB}$, $I_{bound} = 5 \text{ µA}$, $f_{bound} = 5 \text{ MHz}$, $PM_{bound} =$ 70° . For our high-complexity group, we set $G_{bound} = 70 \text{ dB}$, $I_{bound} = 10 \text{ µA}$, $f_{bound} = 20 \text{ MHz}$, $PM_{bound} = 70^{\circ}$. We set $w_G = 3$, $w_f = w_{PM} = 1$, and $w_I = -1$ for the FoM objective function. These parameters are specifically chosen by circuit experts to be challenging for most amplifiers to rigorously evaluate the capabilities of the optimization algorithms.

Baselines and Implementation: We utilize Cadence Spectre to run our simulations. Primarily, we compare our approach against the pure TuRBO optimizer [15] which is proposed for automated analog sizing in [3], and also used for subspace sampling in [19]. TuRBO is run for 1200 steps (BO-1200), matching our method's maximum allowable evaluation budget (200 steps for calibration point synthesis and 100 optimizer steps \times 10 LEDRO iterations). As a stronger baseline, we also compare with an over-optimized TuRBO run with an evaluation budget of 2000 steps (namely BO-2000). For a fair comparison, we ensure that LEDRO and the TuRBO baseline use the same starting points by continuing to train TuRBO using the initial 200 steps used for calibration point synthesis in LEDRO. We also include a Reinforcement Learning (RL) baseline, which was also run for 1200 and 2000 steps (namely RL-1200 and RL-2000). For this baseline, we modify the base model from [4], with the recent improvements of actor-critic networks of [16], [17]. We provide the actor with the region

TABLE I AVERAGE FIGURE OF MERIT AND OPTIMIZATION STEPS FOR LOW-COMPLEXITY AND HIGH-COMPLEXITY OP-AMPS.

	Low-Complexity				High-Complexity			
Algorithm	7nm	10nm	14nm	16nm	7nm	10nm	14nm	16nm
	A	NG FIG	URE OF	Merit	(FoM)	\uparrow		
RL-1200	-1.79	-1.73	-1.76	-1.82	-2.69	-2.64	-2.27	-2.24
RL-2000	-1.72	-1.68	-1.74	-1.80	-2.62	-2.55	-2.20	-2.13
BO-1200	-1.57	-1.48	-1.57	-1.61	-1.46	-1.26	-1.18	-1.16
BO-2000	-1.57	-1.47	-1.47	-1.55	-1.19	-1.21	-1.12	-1.08
LEDRO	-1.45	-1.32	-1.28	-1.25	-0.53	-0.62	-0.61	-0.64
% boost over BO-2000	8%	10%	13%	20%	55%	48%	45%	41%
Av	'G NUM	BER OF	STEPS 7	TO BEST	BO-20	000 FoN	√ I	
BO-2000	680	1030	970	1040	992	1217	1042	875
LEDRO	440	440	390	460	417	675	575	750

of operation knowledge and the critic with additional v_{gs} , v_{ds} , g_m , and i_{ds} information for better optimization. Simulationbased approaches like genetic algorithms [7], [27] are sampleinefficient and poor in performance compared to TuRBO, as shown in [3], [4]. Also, the code for other LLM approaches like [10], [12] is not public and difficult to implement. Thus, we exclude such baselines for our comparisons.

B. Results

We show a detailed breakdown of the performance and efficiency for each amplifier topology and technology node in Fig 7 and Fig 8 for the low-complexity and high-complexity groups, respectively. We notice a clear trend wherein our model LEDRO not only achieves the best FoM performance but also reaches optimal points in lesser number of steps. Through Table 1, we present a summary of the average maximum FoM achieved across the low and high-complexity groups of amplifier designs across the different technology nodes. Our results show the 8-20% and 16-21% improvement



Fig. 8. Performance (FoM) and Efficiency (number of steps) comparison of LEDRO with other baselines for different high-complexity amplifier topologies across four different technology nodes. As shown, LEDRO not only achieves better FOM, but also takes fewer steps to reach the best BO-2000 FoM.



Fig. 9. Average percentage improvement in gain for both sets of amplifiers across technology nodes.

in amplifier performance for low-complexity Op-Amps compared to the 2000-step TuRBO and 2000-step RL optimization, respectively, across technology nodes. These improvements are further amplified in the high-complexity Op-Amps with 41-55% improvement over TuRBO-2000 and 70-80% over RL-2000. Notably, this increased improvement from low to high-complexity is consistently observed across all technology nodes. Such consistency suggests that while low-complexity and low-dimensional circuits are easy to optimize even with more simplistic methods, designing higher-complexity circuits is still challenging for conventional optimization algorithms. On the other hand, our method LEDRO leverages LLMs to reduce and refine the high-complexity search space and efficiently use optimization on this lower-complexity refined space to provide strong improvements for the high-complexity circuits as well. Such results highlight the robustness, generalizability, and scalability of LEDRO.

We also compare the optimization speed in terms of number of steps required by LEDRO and the best baseline BO-2000 to achieve the best FoM achieved by the BO-2000 algorithm, as shown in Table I. Results show that LEDRO achieves an average speed-up of $1.54 \sim 2.48 \times$ across low-complexity Op-Amps and $1.17 \sim 2.38 \times$ for high-complexity Op-Amps across the technology nodes relative to the BO-2000 baseline. This demonstrates the superior optimization efficiency of LEDRO compared to traditional optimization techniques.

C. Analysis: Op-Amp gain (G) improvement

When we examine the detailed improvements introduced by LEDRO, it is remarkable that LEDRO not only enhances the overall FoM, but also demonstrates exceptional efficiency in improving the Op-Amp gain. The average improvement in terms of gain achieved by LEDRO relative to BO-2000 is plotted in Fig. 9. It is noteworthy that the gain improvement is particularly significant for high-complexity circuits across different technology nodes, highlighting the advantage of using LEDRO in design automation. The gain values were capped at G_{bound} if either of the methods met the boundary gain value, ensuring a fair comparison. Overall, LEDRO provides an average improvement of about 15-23% on high-complexity Op-Amps and about 3-6% on low-complexity Op-Amps.

IV. CONCLUSION

In this paper, we introduce LEDRO, which leverages LLMs in synergy with optimization techniques to efficiently explore design space of Op-Amps. Our method advances analog circuit design automation by iteratively refining the design search space through the LLM's prior knowledge and reasoning, thus facilitating strong optimization performance and better designs without human expertise. Experiments across a wide range of topologies and technology nodes demonstrate LEDRO's generalizability with 13-48% FoM improvements and efficiency with $1.7-2.15 \times$ speed-ups compared to conventional optimization techniques. Furthermore, LEDRO is significantly stronger in designing high-complexity and high-dimensional circuits, which provides promise for more practical use cases. In conclusion, the generalizability and adaptability with other optimization techniques marks an advancement in the field, offering a solution for complex analog circuit design challenges.

ACKNOWLEDGMENT

The work was supported by the MIT-IBM Watson AI Lab, and we thank them for their support.

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