

A 2×2 quantum dot array in silicon with fully tuneable pairwise interdot coupling

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Recent advances in semiconductor spin qubits have achieved linear arrays exceeding ten qubits. Moving to two-dimensional (2D) qubit arrays is a critical next step to advance towards fault-tolerant implementations, but it poses substantial fabrication challenges, particularly because enabling control of nearest-neighbor entanglement requires the incorporation of interstitial exchange gates between quantum dots in the qubit architecture. In this work, we present a 2D array of silicon metal-oxide-semiconductor (MOS) quantum dots with tunable interdot coupling between all adjacent dots. The device is characterized at 4.2 K, where we demonstrate the formation and isolation of double-dot and triple-dot configurations. We show control of all nearest-neighbor tunnel couplings spanning up to 30 decades per volt through the interstitial exchange gates and use advanced modeling tools to estimate the exchange interactions that could be realized among qubits in this architecture. These results represent a significant step towards the development of 2D MOS quantum processors compatible with foundry manufacturing techniques.

I. INTRODUCTION

Recent research efforts have already demonstrated significant progress in semiconductor-based spin qubits, showcasing high-fidelity operations^{1–6}, high temperature operations^{7–11}, as well as increasing qubit counts from devices made in both academic¹² and foundry¹³ cleanrooms. One key advantage of a silicon-based platform is the ability to leverage the semiconductor advanced manufacturing capabilities to scale up the number of qubits to millions for a utility-scale quantum computer.

Most of these results have, however, been reported in linear qubit arrays with the current record lying at 12 spin qubits measured in a linear 12-dot device¹³. Advancement from 1D to 2D arrays of quantum dots is necessary for the development of universal quantum computing architectures compatible with error correction methods such as surface code¹⁴. Recent proposals indicate that a $2 \times N$ quantum dot array is enough for a first implementation of error correction¹⁵, considering that one of the rows is integrated by physical qubits while the second row enables entanglement via spin-shuttling.

Two-dimensional arrays of semiconductor quantum dots have been implemented in technologies based on heterostructures in GaAs¹⁶, Si/SiGe^{17,18} and Ge/SiGe^{19–22}. Whilst there have also been demonstrations in silicon MOS, so far they have lacked the tunnel coupling controllability^{23–25}, which is necessary for optimal Pauli-spin readout and for controlling nearest neighbour entanglement via exchange interactions⁶. Modern devices use interstitial exchange gates for this purpose²⁶, however the smaller gate-pitches impose challenges to the fabrication of these devices in academic cleanrooms and in semiconductor foundries²⁷.

Here, we report the fabrication and measurement of a 2×2 quantum dot array in a silicon MOS architecture

with integrated interstitial exchange gates in between adjacent quantum dot pairs (Fig. 1(a)). We characterize quantum dot formation at 4.2 K and demonstrate double dot and triple dot configurations in the device. We also demonstrate tunable tunnel coupling between all pairs of nearest neighboring dots. Based on these results and further modeling and simulation, we provide valuable insights into the development of 2D spin qubit architectures.

II. DEVICE DESIGN AND FABRICATION

Figure 1(a) is a scanning electron micrograph (SEM) of a device nominally identical to the one measured in this work. The device consists of a four-layer aluminum gate stack^{28,29}, fabricated using electron beam lithography (EBL), thermal deposition of Al and lift-off, on top of thermally-grown high-quality SiO₂ on a ^{nat}Si substrate. Aluminum oxide, Al_xO_y is formed at each layer to electrically isolate the subsequent layer of Al gates. Figure 1(b) shows the schematic of laying different gates at each layer forming a gate-stack of 2×2 quantum dots with a single-electron transistor (SET). Starting from layer 1 (yellow), we define quantum dot confinement gates (LCB and RCB), SET barrier gates (SLB and SRB), and a barrier gate between dot 2 and dot 3 (J23). Layer 2 (red) consists of plunger gates (P1, P2, P3 and P4), reservoir gate (RG) and an SET top gate (ST). Layer 3 (blue) comprises barrier gates (J12 and J34), reservoir barrier gates (RESB) and an SET barrier gate (SETB). The uppermost layer (purple) consists of a barrier gate (J41) and an on-chip microwave line (ESR). The ESR line is not used in this work. The Al metal thickness on Layers 1, 2, 3 and 4 are 16, 28, 29 and 100 nm, respectively.

In this design, we define all four plunger gates in the

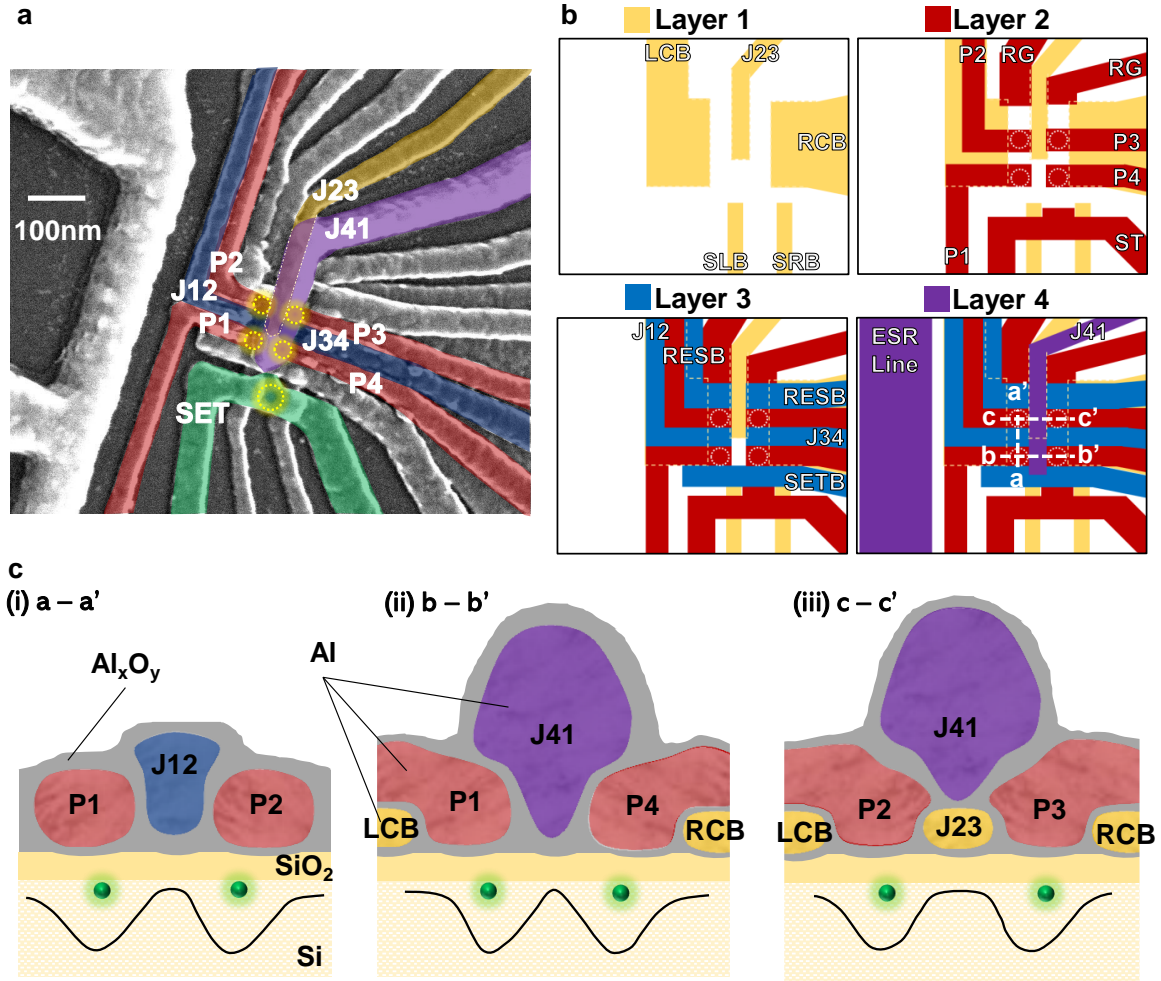


FIG. 1. Device architecture overview. (a) False-coloured SEM image of an identical device used in the experiment. Four quantum dots are formed under respective P1–P4 gates with four individual J-gates to control the interdot coupling between pairs of dots. A single-electron transistor (SET) is fabricated nearby to detect the charge occupancy in the dots. (b) Schematic representation of the multi-level gate stack device, illustrating the layering of gates in order. (c) Schematic cross-section of the device showing the position of a barrier gate (J12, J41 and J23) fabricated in between two plunger gates, as indicated by the white dashed lines in (b). The geometry of the barrier gates has a strong influence on the conduction band profiles.

same layer but J-gates are defined in different layers. This allows us to investigate the influence of J-gate on interdot tunnel coupling based upon its geometry. Figure 1(c) illustrates the cross-sectional schematics of the possible J-gate geometries. From previous transmission electron microscopy (TEM) analyses of multiple device geometries^{6,30,31}, we see the following trends in gate layer stacking. As shown in Fig. 1(c)(i), J12 (also J34) is fabricated in the ~ 20 nm gap between the adjacent plunger gates and hence forming a slightly rounded profile on the gate oxide. In comparison, J41 in Fig. 1(c)(ii) is formed with a slightly pointed profile on top of the gate oxide. On the other hand, J23 is fabricated in layer 1, making it a relatively larger barrier gate (~ 30 nm). The geometry and position of the J-gates will have a strong influence on the conduction band profiles, as indicated in Fig. 1(c).

The RG gates extend over a phosphorus doped region (not shown here) to allow the accumulation of electron layers when a positive voltage, above threshold, is applied. This forms the source of electrons to be loaded into the quantum dots underneath the P1, P2, P3 and P4 gates to form a 2×2 quantum dot array. Both RESB gates act as tunnel barriers for loading of electrons from the reservoirs to the P2 and P3 dots. The J-gates are used to control the interdot tunnel coupling between the four quantum dots. For instance, J12 controls the coupling between P1 and P2 dots while J23 controls the coupling between P2 and P3 dots.

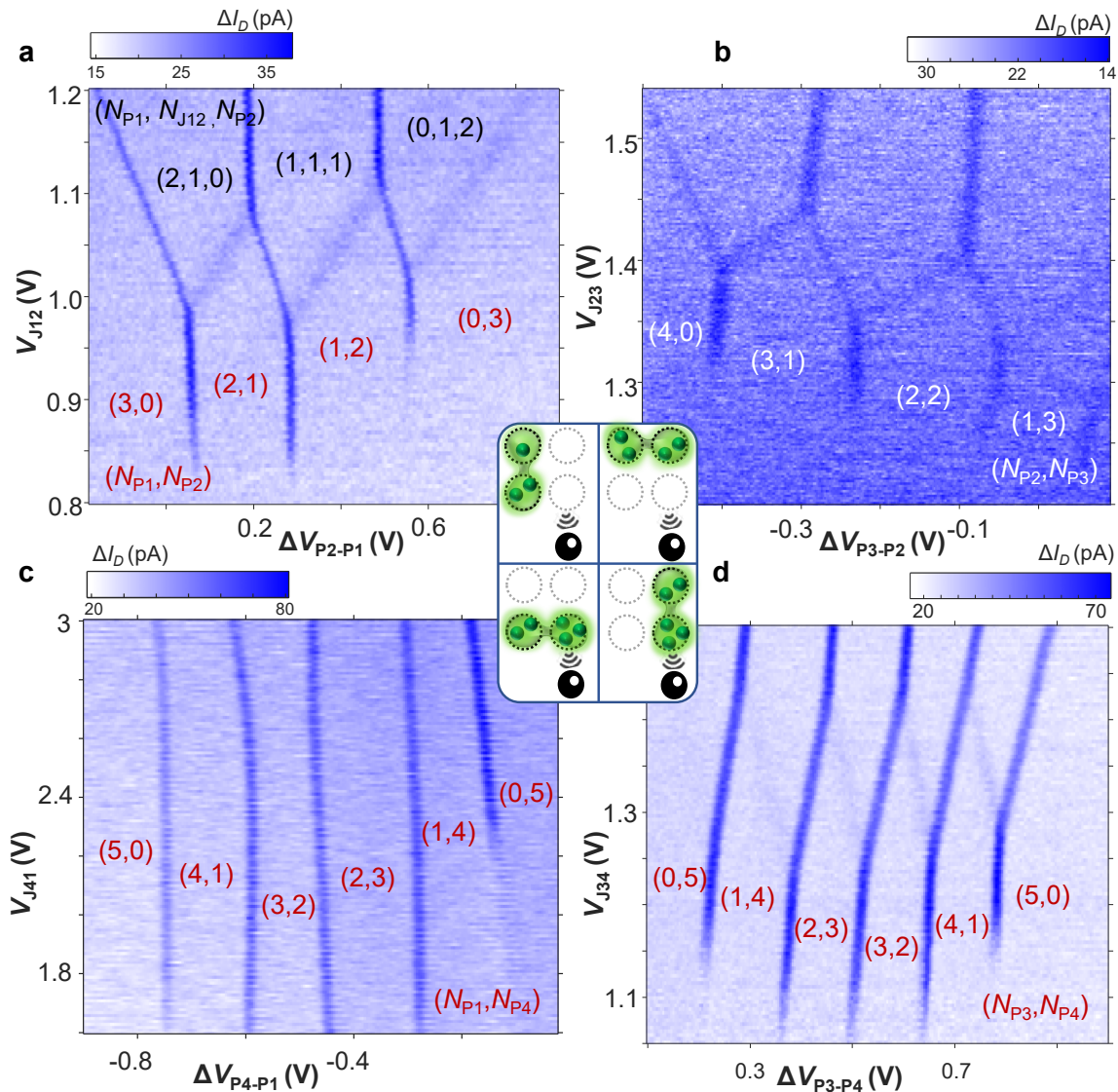


FIG. 2. Isolated-mode charge stability diagrams for a 2×2 quantum dot array system showing the electron occupancy on each pairwise dots. The measured differential current, ΔI_D is obtained from the SET charge sensor as a function of J-gate voltage, V_J and plunger gate detuning voltage, ΔV_P . Each line in the stability diagram indicates a charge transition when an electron tunneling event occurs between the pairwise dots. (a) Charge stability diagram for the P1–P2 pairwise dots showing the electron occupancy on dot P1 and P2 in (N_{P1}, N_{P2}) . Three electrons were loaded into the double dots formed under gates P1 and P2. At low V_{J12} voltage ($< 1V$), a double dot is formed and the electrons are loaded from P1 to P2 dots, one by one as the detuning voltage ΔV_{P2-P1} is increased. At $V_{J12} > 1V$, gate J12 forms a dot underneath and a triple quantum dot charge configuration is measured, with their electron occupancy indicated in $(N_{P1}, N_{J12}, N_{P2})$. Similarly, (b), (c) and (d) show the charge stability diagram for P2–P3, P1–P4 and P3–P4 pairwise dots, respectively.

III. DOUBLE DOT CHARGE CHARACTERISTICS

In this section, we present the electrical measurement of the 2D array of quantum dots sensed via an SET charge sensor at 4.2 K. We use a gate-pulsed lock-in charge sensing technique³² to characterize the charge transitions and electron occupancy of each quantum dot in isolated-mode operation^{8,33}. In isolated mode, the

RESB and RG gate voltages are reduced to below threshold after the dots are loaded with the desired number of electrons in order to pinch off the tunnel rates to the electron reservoir.

Figure 2 shows the charge stability diagrams of the 2×2 quantum dot array for (a) P1–P2, (b) P2–P3, (c) P1–P4 and (d) P3–P4 pairwise dots. The lines in the stability diagram are charge transitions when electron tunneling events occur between the pairwise dots. Between the transition lines, the number of electrons in each

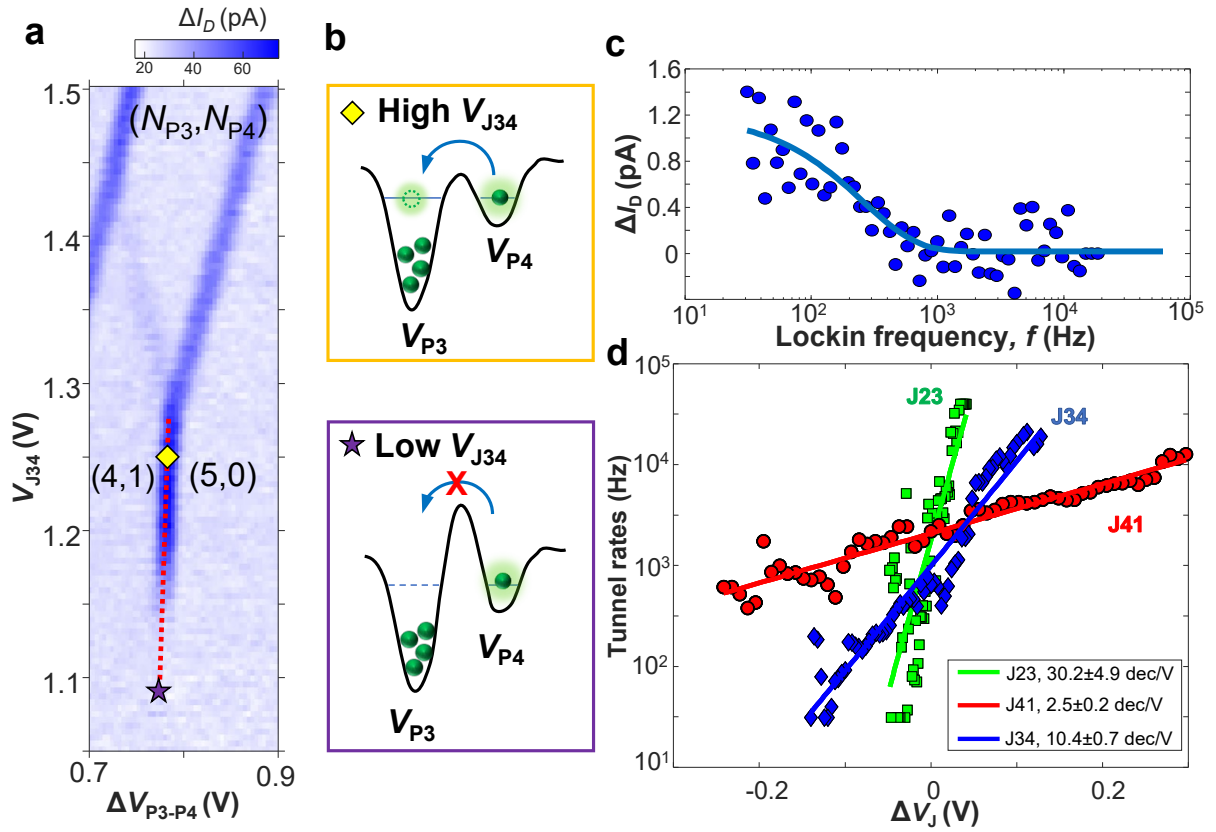


FIG. 3. Tunnel rates measurement between pairwise dots as a function of J-gate voltage, V_J . (a) Focused region of Fig. 2(d) showing the electron transition of P3–P4 dots in the (4,1)–(5,0) electron configuration. (b) Schematic showing the conduction band profiles for P3–P4 dots at high and low J34 voltages. (c) Measurement of the SET differential current, ΔI_D as a function of the gate-pulsed lock-in frequency, f from 31 Hz–61 kHz to probe the electron tunnel rates between P3–P4 dots along the transition line, as indicated by the red dashed line. (d) Tunnel rates as a function of ΔV_J . The rate of increase of tunnel rates is shown in the legend.

P dot is fixed and stipulated as N_P . In Figure 2(a), three electrons are loaded into the double dots formed under gates P1 and P2. Their electron occupancy is indicated in (N_{P1}, N_{P2}) . At low V_{J12} (< 1 V), a double dot is formed and the electrons are shuttled from P1 to P2 dots, one by one, as the detuning voltage ΔV_{P2-P1} is increased. As V_{J12} is further reduced, the barrier between P1 and P2 dots increases resulting in lower tunnel rates and hence the sensing signal ΔI_D diminishes. Conversely, when we further increase V_{J12} (> 1 V in this case), instead of creating a tunnel barrier, an unintended dot is created under the J12 gate. At this point, we form a triple quantum dot system $(N_{P1}, N_{J12}, N_{P2})$ where the tunnel barriers in between P1, J12 and P2 are caused by the thin layer of Al_xO_y .

It is worth noting that the formation of J-dots is also observed under J23 (Fig. 2(b)) and J34 (Fig. 2(d)), but not J41 (Fig. 2(c)). This is owing to the geometry and position of J41 being narrower and defined higher up in the stack compared to other J-gates. Also, a closer look into Fig. 2(b) reveals that J23, being defined in the first layer, actually forms a dot underneath easily with a rel-

atively small increase in voltage.

The four measurements in Fig. 2 were performed with similar SET settings. In these measurements, we can compare the charge sensing signals as a function of pairwise double dot orientation and distance from the SET (see Figure 2 center inset). From deducing the charge transition visibility, we find that the charge sensor has the best sensitivity on the nearest P3–P4 dots and worst sensitivity on the farther P2–P3 dots. Moreover, the SET is most sensitive to inter-dot tunneling events between dots when they (P1-P2 and P3-P4) are positioned perpendicular to the sensor axis (direction of current flow), as compared to parallel (P2-P3 and P1-P4), due to the increased dipole moment when the electron moves toward/away from the SET.

IV. INTER-DOT TUNNEL RATE MEASUREMENTS

To assess the J-gate controllability, we perform pairwise inter-dot tunnel rate measurements. In Fig. 3(a), we

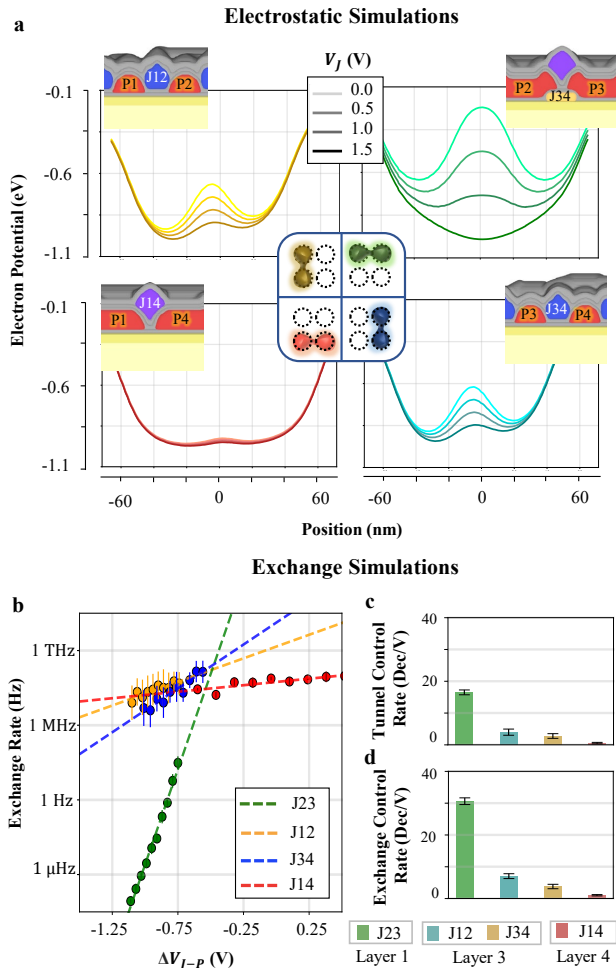


FIG. 4. Modelling of exchange coupling in the 2×2 dot array. (a) Electron potential simulation using COMSOL for different double quantum dot pairs as indicated in the inset cartoons and schematic. The electric potentials are simulated with varying J-gate voltage. (b-d) Path integral Monte Carlo simulations of: (b) Exchange couplings as a function of J-gate biasing. $V_{J-P} = V_J - V_P$, where V_P is the mean bias of the plunger gates defining the dots. (c) Tunnel control rate by each J-gate in dec/V (d) Exchange control rate by each J-gate in dec/V.

focus on the $(4,1)-(5,0)$ electron transition of the P3–P4 double dot charge stability diagram. Figure 3(b) illustrates the conduction band profiles for P3–P4 dots at high and low V_{J34} voltages. At low V_{J34} (purple star), J34 forms a high tunnel barrier and prevents the electron tunneling between the P3 and P4 dots. The charge transition is barely visible indicating that the tunnel rate is significantly smaller than the excitation frequency applied to the gate. As V_{J34} increases, the tunnel barrier decreases and the likelihood of an electron tunneling event occurring between the dots increases. At high V_{J34} (marked yellow square), the tunnel barrier is low and it allows the transfer of electrons between the dots. Thus, a clear

charge transition line is observed.

To probe the inter-dot tunnel rates, we measure the SET differential current, ΔI_D as a function of gate-pulsed lock-in excitation frequency, f , along the charge transition line, as indicated by the red dashed line in Fig. 3(a). Figure 3(c) shows an example of ΔI_D vs excitation frequency, f , at $V_{J34} = 1.208$ V after removing the ac coupling effects between the setup lines. Then, we fit ΔI_D as an exponentially decaying form of $\Delta I_D(f) = I_D \exp\left[-\left(\frac{f}{r}\right)^n\right]$ where r is the electron tunnel rates. We repeat the same measurement on J23, J34 and J41 by sweeping excitation frequencies and their voltages along the corresponding transition lines, ΔV_J , and fit the tunnel rates as plotted in Fig. 3(d). The tunnel rates depend exponentially on the J-gate voltages. J23, being the wider gate and fabricated in layer 1, has the largest controllability on the tunnel rates between P2–P3 dots with a rate of change of 30.2 ± 4.9 dec/V. In contrast, J41, being fabricated in the last layer and having a pointed profile at the bottom, has the weakest influence on the tunnel rates between P1–P4 dots, at a rate of 2.5 ± 0.2 dec/V.

The variations in the J-gate controllability of the tunnel rate in Fig. 3(d) provide an indication of their potential effectiveness in tuning entanglement between spin-qubit pairs formed in the same dots. The exchange rate J is related to the tunnel rate t as

$$J \approx \frac{-4t^2}{U}, \quad (1)$$

where U denotes the Coulomb repulsion. The dependence of both variables under a bias from the exchange gate V_J follows an exponential trend, such that

$$\frac{d \log_{10}(J)}{dV_J} = 2 \frac{d \log_{10}(t)}{dV_J}. \quad (2)$$

From the tunnel control rates $\frac{d \log_{10}(t)}{dV_J}$ measured in Fig. 3(d) of 2.5 dec/V for J41, 10.4 dec/V for J34, and 30.2 dec/V for J23, we can expect exchange rates of 5, 21 and 60 dec/V respectively. Typically an exchange control rate $\frac{d \log_{10}(J)}{dV_J}$ higher than ~ 8 dec/V is desirable in order to be able to switch entanglement on and off despite the presence of random sources of variability (e.g. charge traps, Si/SiO₂ roughness, etc.)³¹. Under these assumptions, only J41 would fall below that threshold for a suitable J-gate design.

V. EXCHANGE MODELLING

The key feature inducing the variations in the tunnel rate control (and the expected exchange rates) is that the J-gates are defined in different metalization layers (See Fig. 1(b)). Each additional metal layer is encapsulated by a thin film of aluminum oxide, which increases their separation from silicon substrate where the dots are

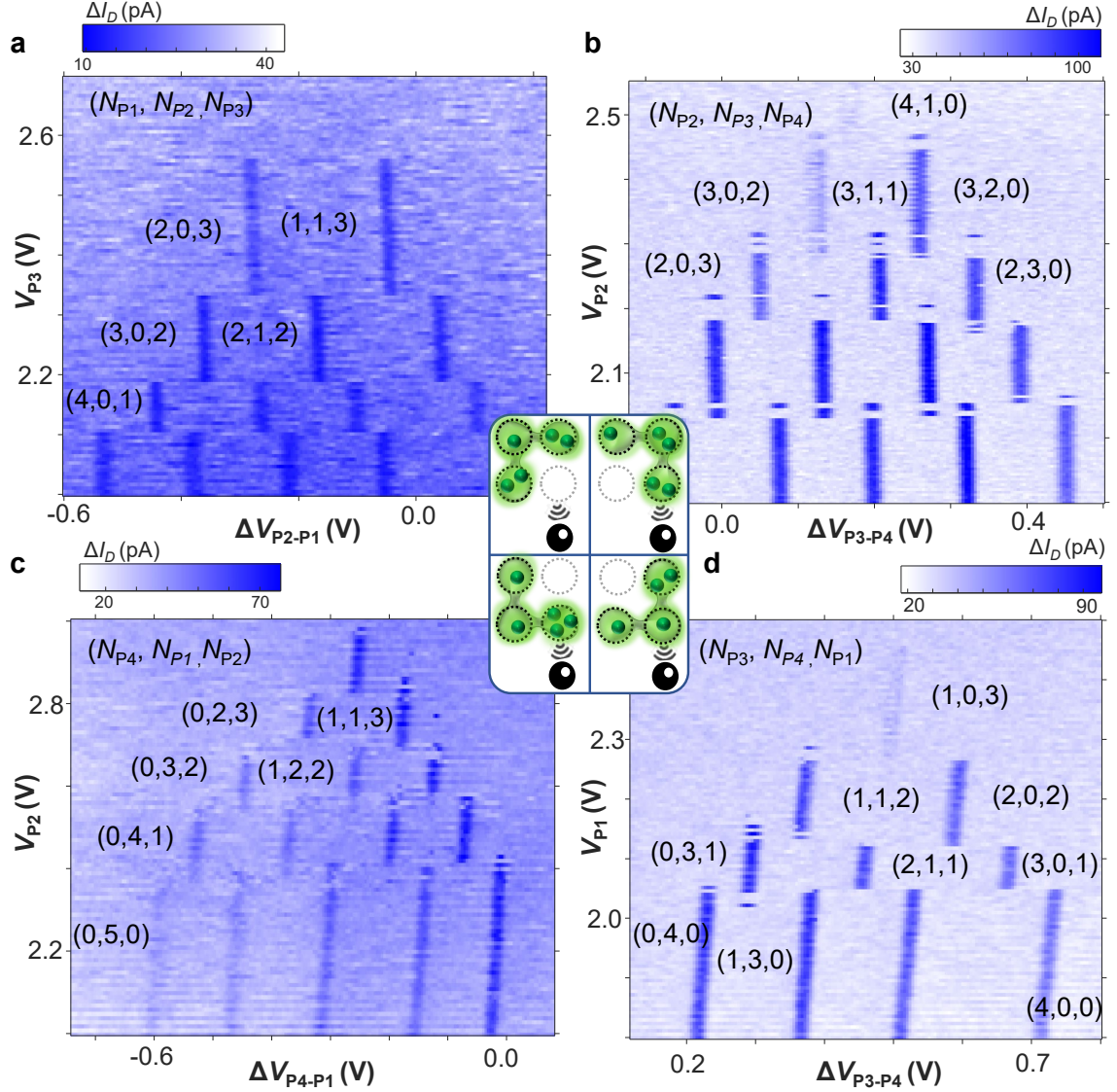


FIG. 5. Isolated-mode triple dot charge stability diagrams in four different configurations. Triple dot system of (a) P1–P2–P3, (b) P2–P3–P4, (c) P4–P1–P2, and (d) P3–P4–P1. Dots in operation are indicated in the inset. The electron occupancy on each dot is denoted as N_P .

Exchange Gate	J23	J12	J34	J14
Metalization Layer	1	3	3	4
Measured Tunnel C. R.	30	10.4	-	2.5
Expected Exchange C. R.	60	21.8	-	5
Simulation Tunnel C. R.	16	4	3	0.5
Simulation Exchange C. R.	31	7	4	1

TABLE I. Comparison of measured and simulated control rates on each J-gate. Units are in decades per volt. The experimental control rate is projected from the measured control rate using equation (2).

formed, thus systematically reducing their effectiveness.

We support this statement with finite element simulations of the electrostatic potential in Comsol Multiphysics, following the methods presented in Ref.[31]. We show in Fig. 4(a) that J23 (in layer 1) has the strongest control of the inter-dot potential, as it is the closest to the Si/SiO₂ interface, while J14 (in layer 4) is the least effective. We simulate tunnel and exchange rates with a path integral Monte Carlo approach³⁴ (see Fig. 4(b–d)), observing a similar trend as the tunnel rates measured in Fig. 3(d). Figures 4(c–d) clearly show that both tunnel and exchange control rates decrease with the metalization layer.

Despite having a good qualitative agreement, the simulated tunnel control rates are significantly smaller than in experiments (Table IV). This is most likely due to limita-

tions in reproducing the device geometry accurately (gate shape, granularity, variations in the oxide thickness, etc.). Modeling could be improved for future studies by carefully analyzing these features with TEM images of the transversal cuts of the device and integrating them into the 3D digital model³¹.

VI. TRIPLE DOT CHARGE CHARACTERISTICS

In addition to double dot configurations, we are also able to tune the device into triple dot configurations. Figure 5 shows the four charging maps of isolated mode triple dot systems in (a) P1–P2–P3, (b) P2–P3–P4, (c) P4–P1–P2, and (d) P3–P4–P1. The number of electrons occupying each dot is indicated by N_P . In the P3–P4–P1 triple dot system (see Fig. 5(d)), we first load four electrons into the P4 dot and form a (0,4,0) charge configuration at the bottom left of the plot. By increasing the detuning voltage ΔV_{P3-P4} , we move electrons one by one into the P3 dot, from (0,4,0) to (1,3,0), through to (4,0,0). Similarly, by increasing the voltage on P1, we can move electrons one by one into the P1 dot, from (4,0,0) to (0,0,4). Note that the horizontal charge transitions are hardly visible because the tunnel rate between P1 and either of P3 or P4 is much lower than the gate-pulsed excitation frequency. To put it simply, we sweep the detuning voltage of two plunger gates and step the voltage of the third plunger gate, such that the third quantum dot acts as an electron reservoir from (to) where electrons can (un)load, forming the "Christmas tree" charging diagram. The inset in the centre of Fig. 5 illustrates the active triple dots in each measurement plot. Notably, the charge transition visibility is lowest for the P1–P2–P3 triple dot as it is furthest away from the SET. These measurements demonstrate the high tunability and stability of all the four dots in the 2×2 quantum dot array.

VII. CONCLUSION AND OUTLOOK

We have fabricated a 2D array of silicon MOS quantum dot and demonstrated pairwise double-dot and triple-dot arrangements in isolated mode at 4.2 K. With the four-layer gate stack, the device can be operated in the single-electron occupancy regime and possesses excellent tunability. The experiments offer important learnings on (i) the design of J-gate and its tunnel-rate controllability; (ii) the position of SET with respect to dots and its sensitivity and (iii) the characterisation of tunnel rates and its relation to exchange rates. The simulation techniques employed can help with future device design optimisation, ensuring high-level exchange controllability for qubit entanglement. These findings highlight the potential of silicon MOS quantum dots as versatile platforms with excellent controllability and connectivity, paving the

way for advancements in quantum computing and quantum simulation.

DATA AVAILABILITY

The data supporting the findings in this study are available from the corresponding authors upon reasonable request.

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Competing Interests

A.S.D. is the CEO and a director of Diraq Pty Ltd. W.H.L., T.T., A.D., K.W.C, F.E.H., C.C.E., C.H.Y., A.L., A.S. and A.S.D. declare equity interest in Diraq Pty Ltd.

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